

RS18G30 – 16-Phase 3-Output TLVR Controller with SVID, SVI3, AVSBus and PMBus

Features

Flexible Triple-Output Multiphase Control

- Up to 16 total phases ($N+M+O \leq 16$)
- Flexible phase allocation from 16+0+0 to 8+4+4
- Flexible phase ordering
- Designed for use with Reed Smart Power Stages or Smart Power Blocks

Native TLVR & Fast Transient Performance

- Native Trans-Inductor Voltage Regulator (TLVR) support
 - No additional external passive components required
- Integrated 1k Ω current-sense resistor
- Up to 4MHz switching frequency
- Constant-On-Time (COT) control
- Programmable DC load line
- Automatic phase add/drop
- Programmable overshoot and undershoot reduction

Wide Operating Range and High Accuracy

- 4.5V to 16V input voltage range
- 0.2V to 2.7V output voltage range
- $\pm 0.5\%$ output voltage accuracy with differential sensing

Comprehensive protection

- Programmable latch-off or auto-retry fault response
- UVLO, UVP, OVP, OCP, OTP
- Cycle-by-cycle per-phase current limit

SVID, SVI3, AVSBus, PMBus & Diagnostics

- Intel SVID compliant
- AMD SVI3 3.0 compliant
- AVSBus 1.4 / 2.0 compliant
- PMBus 1.4.1 compliant
- Internal compensation
- Multi-Time Programmability (MTP) with up to 31 writes
- Black-box fault-record registers

Package

- 7mm $\times$ 7mm, 60-pin QFN
- RoHS compliant and green

Applications

- AI Accelerators and GPU Core Power
- Server and HPC Processor Core Power
- Graphics Cards
- High-Current Multiphase Voltage Regulators
- Telecom Power Systems

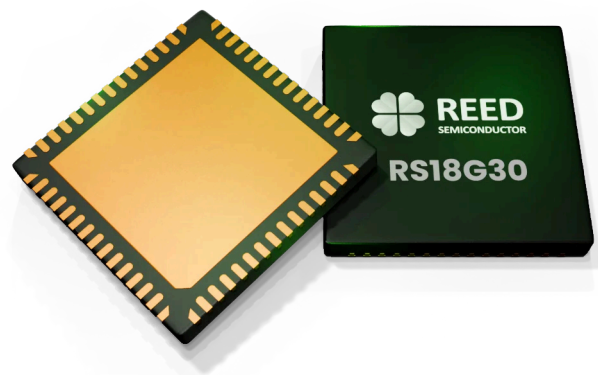
Description

The RS18G30 is a high-performance, 3-output digital multiphase controller supporting up to 16 phases with flexible $N + M + O \leq 16$ phase allocation. Designed for server, computing, graphics, and high-performance power applications, the device supports a 4.5V to 16V input range and 0.2V to 2.7V output range with $\pm 0.5\%$ output voltage accuracy.

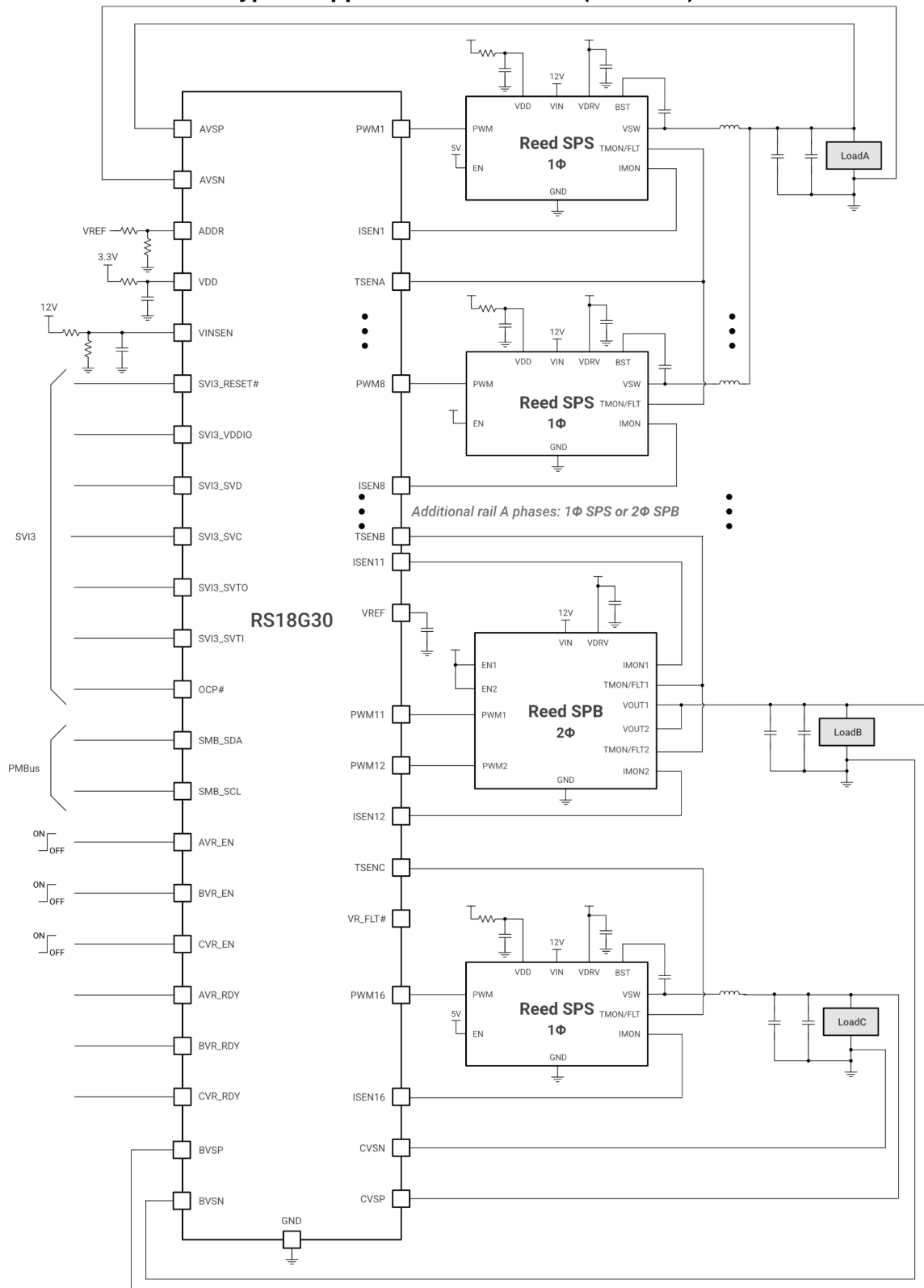
Native TLVR support, Constant-On-Time (COT) control, programmable DC load line, automatic phase add/drop, and operation up to 4MHz enable fast transient response and efficient high-current power conversion. Integrated telemetry provides accurate monitoring of input and output voltage, output current, and temperature.

The RS18G30 supports Intel SVID, AMD SVI3, AVSBus, and PMBus 1.4.1, providing broad platform compatibility along with digital configuration, telemetry, and system monitoring. MTP enables nonvolatile configuration, while black-box registers capture fault information for system diagnostics. Comprehensive protection includes UVLO, UVP, OVP, OCP, OTP, and cycle-by-cycle per-phase current limiting.

Designed to operate with Reed [Smart Power Stages](#) or [Smart Power Blocks](#), the RS18G30 provides a scalable solution for multiple high-current processor rails. The device is available in a 7mm $\times$ 7mm, 60-pin QFN package and operates from -40°C to 125°C .



Typical Application Schematic (8 + 4 + 1)



Ordering Information

PART NUMBER	PACKAGE	SIZE	MSL RATING	SHIPPING METHOD	PACKAGE MARKING
RS18G30R	QFN-60	7 × 7mm	Level-3	3000u Tape & Reel	R18G30

Top Marking

Line 1

- RS: Prefix of Reed Semiconductor (R is replaced by E for engineering lots)
- YY: Year code
- WW: Week code

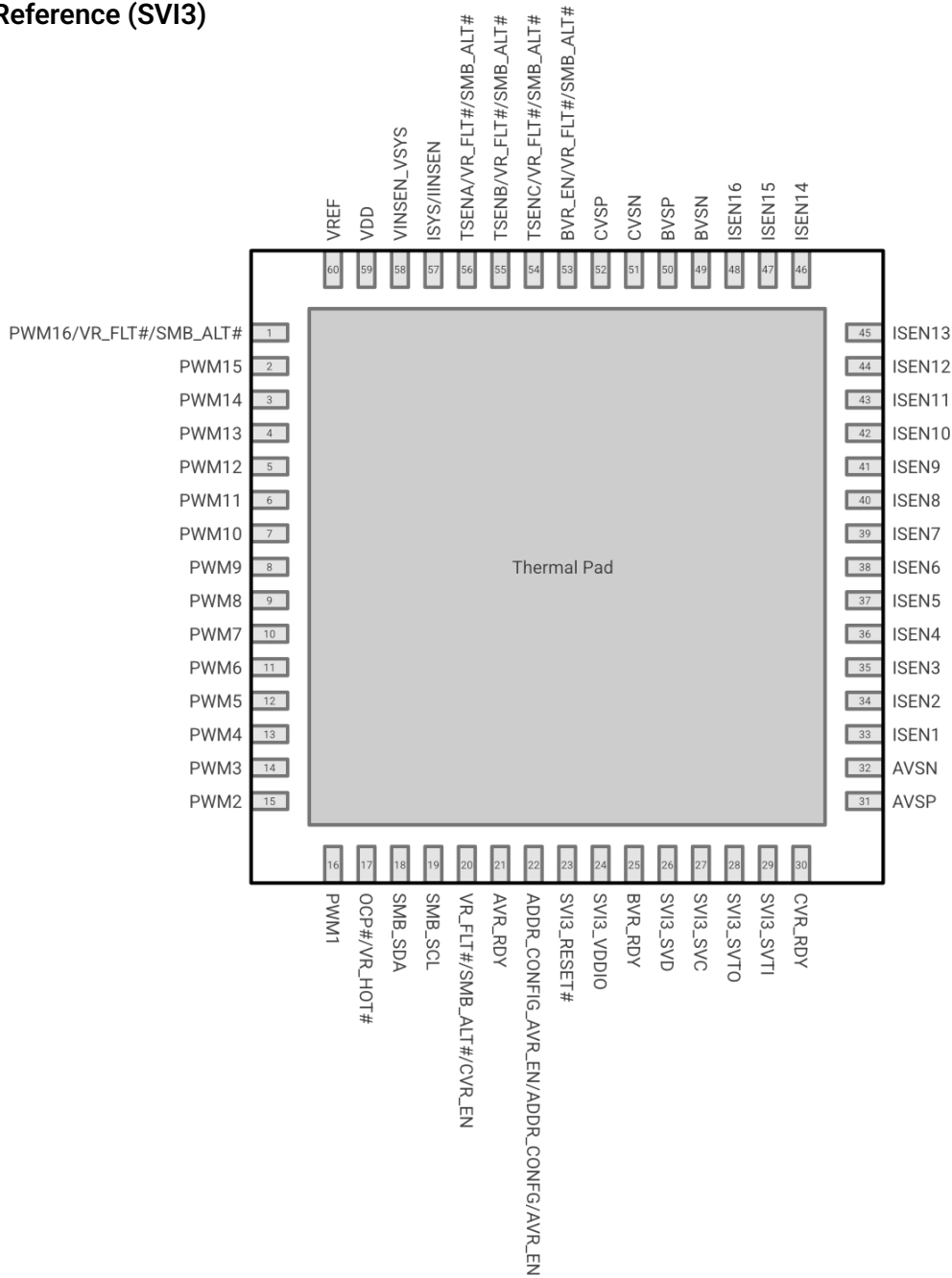
Line 2

- PPPPP: Truncated part number

Line 3

- LLLLL: Lot code
- S: Assembly site code

Package Reference (SVI3)



QFN-60 (7 × 7mm)

Pin Descriptions (SVI3)

PIN	NAME	TYPE	DESCRIPTION
1	PWM16/ VR_FLT#/ SMB_ALT#	O	PWM16 – PWM output for Phase 16. VR_FLT# – Active-low catastrophic fault indicator; controller stops regulating when asserted. SMB_ALT# – PMBus active-low ALERT# signal.
2	PWM15	O	PWM output for Phase 15.
3	PWM14	O	PWM output for Phase 14.
4	PWM13	O	PWM output for Phase 13.
5	PWM12	O	PWM output for Phase 12.
6	PWM11	O	PWM output for Phase 11.
7	PWM10	O	PWM output for Phase 10.
8	PWM9	O	PWM output for Phase 9.
9	PWM8	O	PWM output for Phase 8.
10	PWM7	O	PWM output for Phase 7.
11	PWM6	O	PWM output for Phase 6.
12	PWM5	O	PWM output for Phase 5.
13	PWM4	O	PWM output for Phase 4.
14	PWM3	O	PWM output for Phase 3.
15	PWM2	O	PWM output for Phase 2.
16	PWM1	O	PWM output for Phase 1.
17	OCP#/ VR_HOT#	O	OCP# – Active-low overcurrent warning output; asserts when current exceeds the SVI3 OCP_THRESH or OCP_WARN_THRESH setting. VR_HOT# – Active-low thermal warning output; asserts when temperature exceeds the configured WARN_LIMIT threshold.
18	SMB_SDA	I/O	PMBus bidirectional serial data signal.
19	SMB_SCL	I	PMBus serial clock signal.
20	VR_FLT#/ SMB_ALT#/ CVR_EN	O	VR_FLT# – Active-low catastrophic fault indicator; controller stops regulating when asserted. SMB_ALT# – PMBus active-low ALERT# signal. CVR_EN – Enables Active High Enable for Rail C.
21	AVR_RDY	O	Active-high power-good output; asserts when the output voltage of Rail A is in regulation.
22	ADDR_ CONFIG_/ AVR_EN/ ADDR_/ CONFIG/ AVR_EN	I	ADDR_CONFIG_AVR_EN – Combined ADDR_CONFIG and AVR_EN function; operates as ADDR_CONFIG during VDD ramp-up and as AVR_EN afterward. ADDR_CONFIG – Combined ADDR and CONFIG input; operates as ADDR during VDD ramp-up when the top and bottom resistors are populated, or as CONFIG when the bottom resistor is populated. AVR_EN – Active-high enable input for Rail A.

PWM outputs (Pins 1–16): 3.3V CMOS tri-state outputs. Low: low-side FET ON; High: high-side FET ON; Tri-state: both FETs OFF. If unused, leave floating.

Type: I = Input, O = Output, I/O = Bidirectional, P = Power, G = Ground, – = No Connect.

Pin Descriptions (SVI3)

PIN	NAME	TYPE	DESCRIPTION
23	SVI3_RESET#	I	Active-low SVI3 reset input; resets all SVI3 state machines and SVI3-defined registers to their default states.
24	SVI3_VDDIO	P	SVI3 interface power and voltage-reference input for the SVD, SVTI, and SVTO signals. Connect a ~1µF decoupling capacitor to GND.
25	BVR_RDY	O	Active-high power-good output; asserts when the output voltage of Rail B is in regulation.
26	SVI3_SVD	I	Serial VID Data – Push-pull SVI3 data input that receives commands from the controller.
27	SVI3_SVC	I	Serial VID Clock – Push-pull SVI3 clock input for SVD, SVTI, and SVTO.
28	SVI3_SVTO	O	Serial VID Telemetry Output – Push-pull telemetry output driven by each device; carries telemetry and acknowledge packets.
29	SVI3_SVTI	I	Serial VID Telemetry Input – Telemetry input driven by the next-furthest device from the controller in the telemetry daisy chain; carries telemetry and acknowledge packets.
30	CVR_RDY	O	Active-high power-good output; asserts when the output voltage of Rail C is in regulation.
31	AVSP	I	Rail A positive remote voltage-sense input at the load point.
32	AVSN	I	Rail A negative (GND) remote voltage-sense input at the load point.
33	ISEN1	I	Current-sense input for Phase 1.
34	ISEN2	I	Current-sense input for Phase 2.
35	ISEN3	I	Current-sense input for Phase 3.
36	ISEN4	I	Current-sense input for Phase 4.
37	ISEN5	I	Current-sense input for Phase 5.
38	ISEN6	I	Current-sense input for Phase 6.
39	ISEN7	I	Current-sense input for Phase 7.
40	ISEN8	I	Current-sense input for Phase 8.
41	ISEN9	I	Current-sense input for Phase 9.
42	ISEN10	I	Current-sense input for Phase 10.
43	ISEN11	I	Current-sense input for Phase 11.
44	ISEN12	I	Current-sense input for Phase 12.
45	ISEN13	I	Current-sense input for Phase 13.
46	ISEN14	I	Current-sense input for Phase 14.
47	ISEN15	I	Current-sense input for Phase 15.
48	ISEN16	I	Current-sense input for Phase 16.

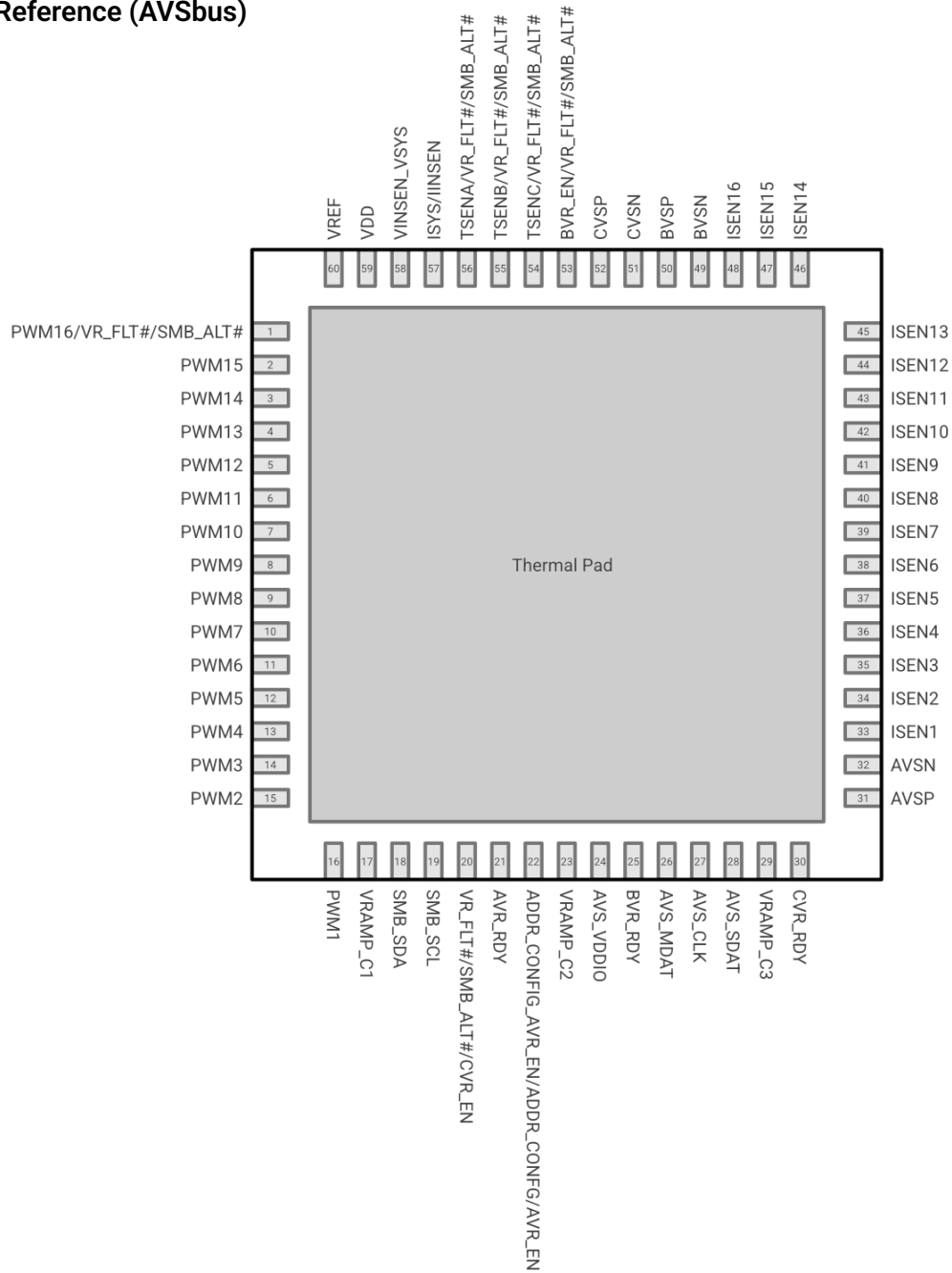
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Pin Descriptions SVI3

PIN	NAME	TYPE	DESCRIPTION
49	BVSN	I	Rail B positive remote voltage-sense input at the load point.
50	BVSP	I	Rail B negative (GND) remote voltage-sense input at the load point.
51	CVSN	I	Rail C positive remote voltage-sense input at the load point.
52	CVSP	I	Rail C negative (GND) remote voltage-sense input at the load point.
53	BVR_EN/ VR_FLT#/ SMB_ALT#	I/O	BVR_EN – Active-high enable input for Rail B. VR_FLT# – Active-low catastrophic fault indicator; controller stops regulating when asserted. SMB_ALT# – PMBus active-low ALERT# signal.
54	TSENC/ VR_FLT#/ SMB_ALT#	I/O	TSENC – Temperature-sense input for all phases of Rail C. VR_FLT# – Active-low catastrophic fault indicator; controller stops regulating when asserted. SMB_ALT# – PMBus active-low ALERT# signal.
55	TSENB/ VR_FLT#/ SMB_ALT#	I/O	TSENB – Temperature-sense input for all phases of Rail B. VR_FLT# – Active-low catastrophic fault indicator; controller stops regulating when asserted. SMB_ALT# – PMBus active-low ALERT# signal.
56	TSENA/ VR_FLT#/ SMB_ALT#	I/O	TSENA – Temperature-sense input for all phases of Rail A. VR_FLT# – Active-low catastrophic fault indicator; controller stops regulating when asserted. SMB_ALT# – PMBus active-low ALERT# signal.
57	ISYS/IINSEN/ PSYS	I	ISYS/IINSEN – Input-current sense; connect a resistor to GND and ensure the pin voltage does not exceed VREF (1.5V). PSYS – Input-power sense; connect a resistor to GND and ensure the pin voltage does not exceed VREF (1.5V).
58	VSYS/ VINSEN	I	VSYS/VINSEN – System/input-voltage sense input. Use a resistive divider (1/6) and a 0.1µF decoupling capacitor to GND. This pin also represents VSYS.
59	VDD	P	3.3V supply input. Connect a ≥1µF decoupling capacitor to GND.
60	VREF	O	1.5V reference-voltage output. Connect a 1µF to 4.7µF decoupling capacitor to GND.
–	Thermal Pad	GND	Ground pad; connect to the GND plane with vias.

Type: I = Input, O = Output, I/O = Bidirectional, P = Power, G = Ground, – = No Connect.

Package Reference (AVSbus)



QFN-60 (7 × 7mm)

Pin Descriptions (AVSBus)

PIN	NAME	TYPE	DESCRIPTION
1	PWM16/ VR_FLT#/ SMB_ALT#	O	PWM16 – PWM output for Phase 16. VR_FLT# – Active-low catastrophic fault indicator; controller stops regulating when asserted. SMB_ALT# – PMBus active-low ALERT# signal.
2	PWM15	O	PWM output for Phase 15.
3	PWM14	O	PWM output for Phase 14.
4	PWM13	O	PWM output for Phase 13.
5	PWM12	O	PWM output for Phase 12.
6	PWM11	O	PWM output for Phase 11.
7	PWM10	O	PWM output for Phase 10.
8	PWM9	O	PWM output for Phase 9.
9	PWM8	O	PWM output for Phase 8.
10	PWM7	O	PWM output for Phase 7.
11	PWM6	O	PWM output for Phase 6.
12	PWM5	O	PWM output for Phase 5.
13	PWM4	O	PWM output for Phase 4.
14	PWM3	O	PWM output for Phase 3.
15	PWM2	O	PWM output for Phase 2.
16	PWM1	O	PWM output for Phase 1.
17	VRAMP_C1	O	Active-low Rail A voltage-ramp status output. Remains high until the commanded VBOOT or VID target is reached.
18	SMB_SDA	I/O	PMBus bidirectional serial data signal.
19	SMB_SCL	I	PMBus serial clock signal.
20	VR_FLT#/ SMB_ALT#/ CVR_EN	O	VR_FLT# – Active-low catastrophic fault indicator; controller stops regulating when asserted. SMB_ALT# – PMBus active-low ALERT# signal. CVR_EN – Enables Active High Enable for Rail C.
21	AVR_RDY	O	Active-high power-good output; asserts when the output voltage of Rail A is in regulation.
22	ADDR_ CONFIG_/ AVR_EN/ ADDR_/ CONFIG/ AVR_EN	I	ADDR_CONFIG_AVR_EN – Combined ADDR_CONFIG and AVR_EN function; operates as ADDR_CONFIG during VDD ramp-up and as AVR_EN afterward. ADDR_CONFIG – Combined ADDR and CONFIG input; operates as ADDR during VDD ramp-up when the top and bottom resistors are populated, or as CONFIG when the bottom resistor is populated. AVR_EN – Active-high enable input for Rail A.

PWM outputs (Pins 1–16): 3.3V CMOS tri-state outputs. Low: low-side FET ON; High: high-side FET ON; Tri-state: both FETs OFF. If unused, leave floating.

Type: I = Input, O = Output, I/O = Bidirectional, P = Power, G = Ground, – = No Connect.

Pin Descriptions (AVSBus)

PIN	NAME	TYPE	DESCRIPTION
23	VRAMP_C2	O	Active-low Rail B voltage-ramp status output. Remains high until the commanded VBOOT or VID target is reached.
24	AVS_VDDIO	P	AVSBus interface supply and I/O reference voltage for AVS_CLK, AVS_MDAT, and AVS_SDAT.
25	BVR_RDY	O	Active-high power-good output; asserts when the output voltage of Rail B is in regulation.
26	AVS_MDAT	I	AVSBus command-data input.
27	AVS_CLK	I	AVSBus serial clock input.
28	AVS_SDAT	O	AVSBus response-data signal.
29	VRAMP_C3	I	Active-low Rail C voltage-ramp status output. Remains high until the commanded VBOOT or VID target is reached.
30	CVR_RDY	O	Active-high power-good output; asserts when the output voltage of Rail C is in regulation.
31	AVSP	I	Rail A positive remote voltage-sense input at the load point.
32	AVSN	I	Rail A negative (GND) remote voltage-sense input at the load point.
33	ISEN1	I	Current-sense input for Phase 1.
34	ISEN2	I	Current-sense input for Phase 2.
35	ISEN3	I	Current-sense input for Phase 3.
36	ISEN4	I	Current-sense input for Phase 4.
37	ISEN5	I	Current-sense input for Phase 5.
38	ISEN6	I	Current-sense input for Phase 6.
39	ISEN7	I	Current-sense input for Phase 7.
40	ISEN8	I	Current-sense input for Phase 8.
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43	ISEN11	I	Current-sense input for Phase 11.
44	ISEN12	I	Current-sense input for Phase 12.
45	ISEN13	I	Current-sense input for Phase 13.
46	ISEN14	I	Current-sense input for Phase 14.
47	ISEN15	I	Current-sense input for Phase 15.
48	ISEN16	I	Current-sense input for Phase 16.

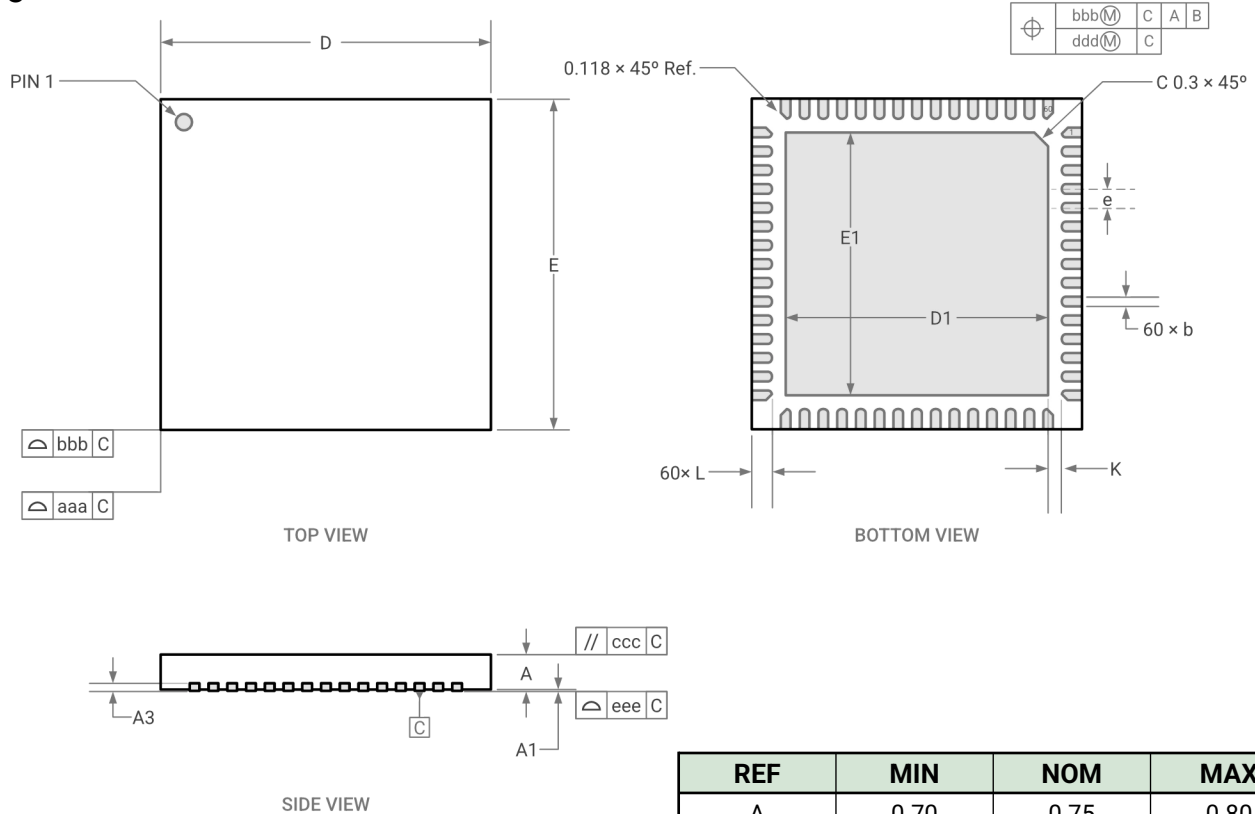
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Pin Descriptions (AVSBus)

PIN	NAME	TYPE	DESCRIPTION
49	BVSN	I	Rail B positive remote voltage-sense input at the load point.
50	BVSP	I	Rail B negative (GND) remote voltage-sense input at the load point.
51	CVSN	I	Rail C positive remote voltage-sense input at the load point.
52	CVSP	I	Rail C negative (GND) remote voltage-sense input at the load point.
53	BVR_EN/ VR_FLT#/ SMB_ALT#	I/O	BVR_EN – Active-high enable input for Rail B. VR_FLT# – Active-low catastrophic fault indicator; controller stops regulating when asserted. SMB_ALT# – PMBus active-low ALERT# signal.
54	TSENC/ VR_FLT#/ SMB_ALT#	I/O	TSENC – Temperature-sense input for all phases of Rail C. VR_FLT# – Active-low catastrophic fault indicator; controller stops regulating when asserted. SMB_ALT# – PMBus active-low ALERT# signal.
55	TSENB/ VR_FLT#/ SMB_ALT#	I/O	TSENB – Temperature-sense input for all phases of Rail B. VR_FLT# – Active-low catastrophic fault indicator; controller stops regulating when asserted. SMB_ALT# – PMBus active-low ALERT# signal.
56	TSENA/ VR_FLT#/ SMB_ALT#	I/O	TSENA – Temperature-sense input for all phases of Rail A. VR_FLT# – Active-low catastrophic fault indicator; controller stops regulating when asserted. SMB_ALT# – PMBus active-low ALERT# signal.
57	ISYS/IINSEN/ PSYS	I	ISYS/IINSEN – Input-current sense; connect a resistor to GND and ensure the pin voltage does not exceed VREF (1.5V). PSYS – Input-power sense; connect a resistor to GND and ensure the pin voltage does not exceed VREF (1.5V).
58	VSYS/ VINSEN	I	VSYS/VINSEN – System/input-voltage sense input. Use a resistive divider (1/6) and a 0.1µF decoupling capacitor to GND. This pin also represents VSYS.
59	VDD	P	3.3V supply input. Connect a ≥1µF decoupling capacitor to GND.
60	VREF	O	1.5V reference-voltage output. Connect a 1µF to 4.7µF decoupling capacitor to GND.
–	Thermal Pad	GND	Ground pad; connect to the GND plane with vias.

Type: I = Input, O = Output, I/O = Bidirectional, P = Power, G = Ground, – = No Connect.

Package Dimensions

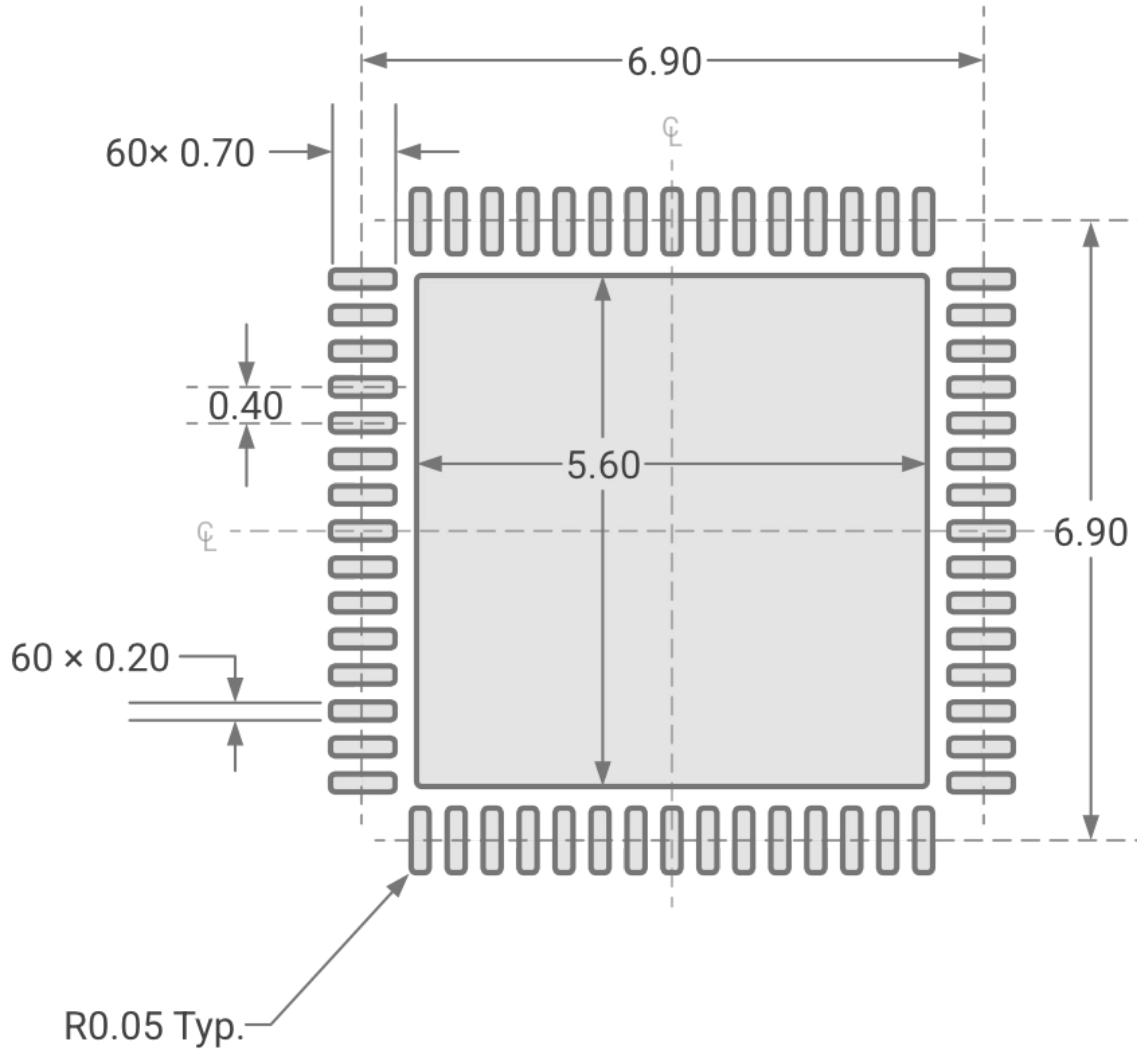


Notes

1. All dimensions are in millimeters.
2. Drawing per JEDEC MO-220.
3. Drawing is not to scale.

REF	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	—	0.05
A3	0.203 Ref.		
D	6.90	7.00	7.10
E	6.90	7.00	7.10
D1	5.55	5.60	5.65
E1	5.55	5.60	5.65
b	0.20	0.225	0.25
e	0.40 BSC		
L	0.35	0.40	0.45
K	0.30 Ref.		
Geometric Tolerancing			
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		

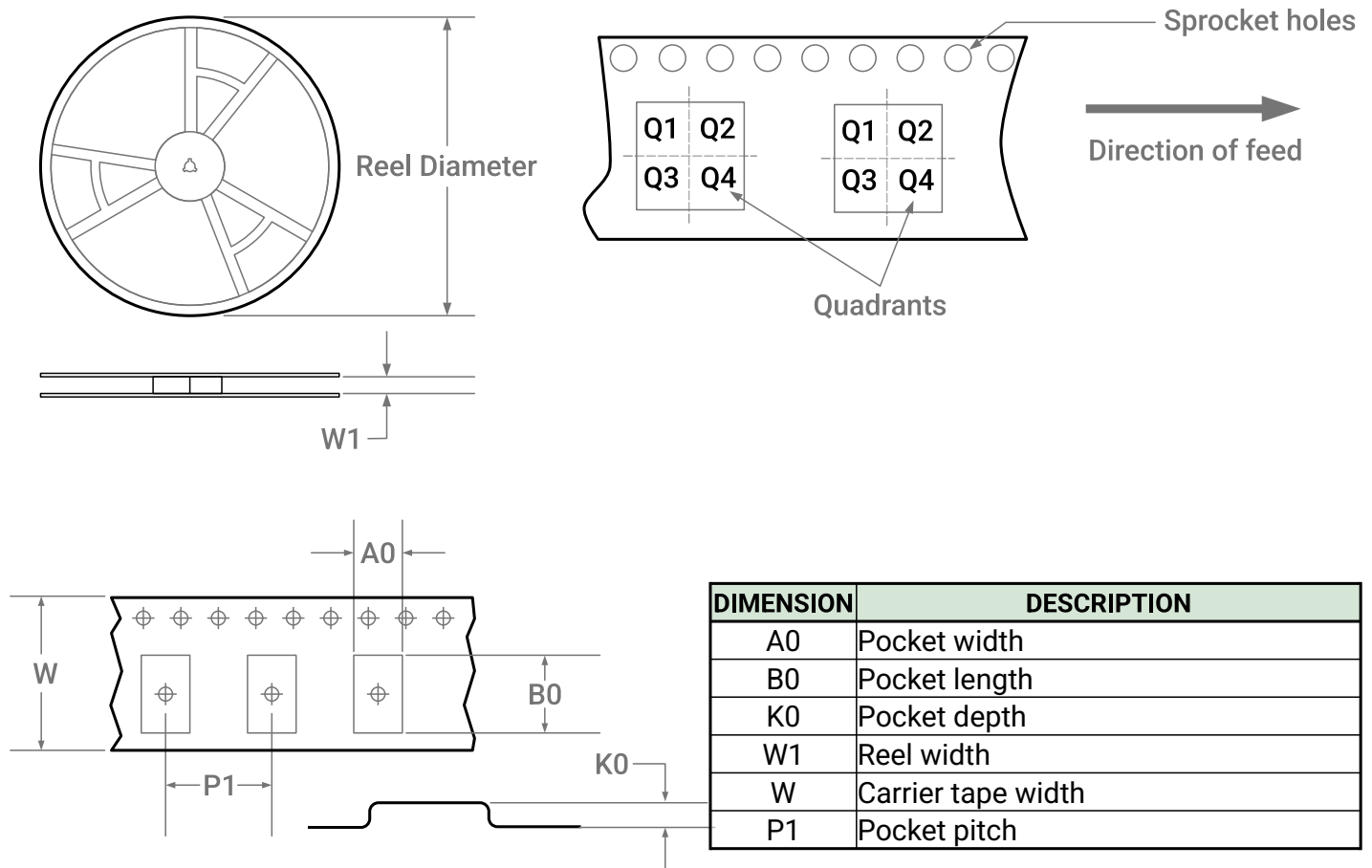
Recommended Land Pattern



Notes:

1. All dimensions are in millimeters.
2. Drawing is not to scale.

Tape and Reel Information

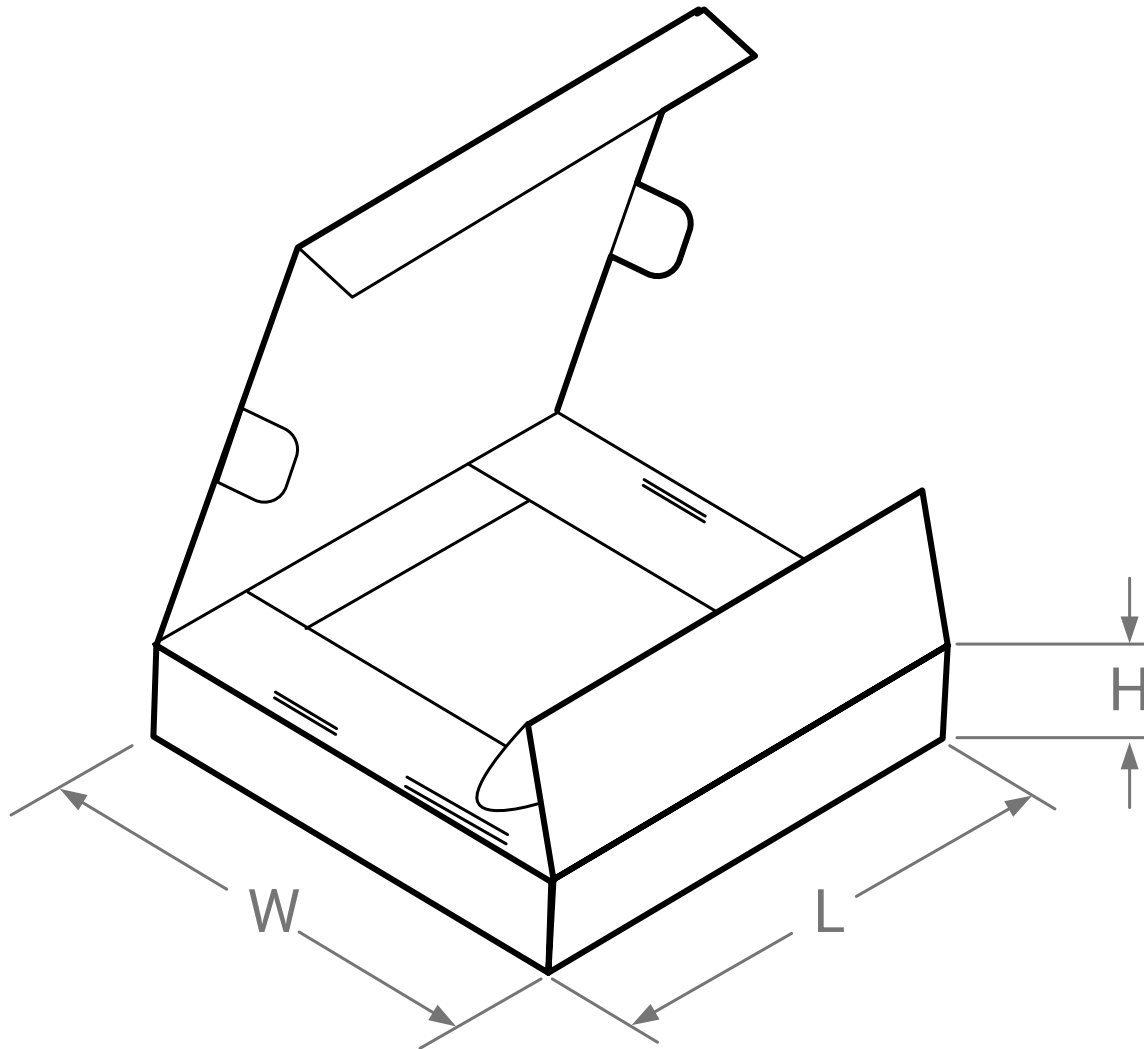


PACKAGE SIZE	REEL DIAMETER	W1	A0	B0	K0	P1	W	QUADRANT
7 × 7	330	16	7.3	7.3	1.1	12	16	Q2

Note:

1. All dimensions are nominal
2. All dimensions are in millimeters (mm)

Pizza Box Dimensions



PACKAGE SIZE	UNITS / BOX	LENGTH	WIDTH	HEIGHT
7 × 7	3000	354	337	55

Notes:

1. All measurements are in millimeters;
2. All measurements are nominal.