RS16630 — 6-Phase Triple-Rail TLVR Controller with AVSBus and PMBus

Features

Flexible 6-Phase Triple-Rail Architecture

- Up to 6 phases with flexible N + M + O ≤ 6 allocation
  - Configurations from 6 + 0 + 0 to 2 + 2 + 2
- Flexible phase-order assignment
- Compatible with Reed Smart Power Stages and Smart Power Blocks

Native TLVR & Fast Transient Performance

- Native Trans-Inductor Voltage Regulator (TLVR) support
  - No additional external passive components required
  - Integrated 1kΩ current-sense resistor
- Programmable overshoot and undershoot reduction
- Automatic phase add/drop with programmable thresholds
- Thermal phase balancing
- Up to 4MHz switching frequency
- Constant-on-time control
- Programmable DC load line

Wide operating range and high-accuracy regulation

- 4.5V to 16V input; 0.2V to 2.8V output
- ±0.5% output-voltage accuracy with differential sensing
- Programmable load-line control

Integrated telemetry

- ±1.5% voltage and current accuracy
- ±2°C temperature accuracy

Comprehensive protection

- UVLO, UVP, OVP, OCP, and OTP
- Cycle-by-cycle per-phase current limiting
- Programmable latch-off or auto-retry fault response

Digital Interfaces, Configuration & Diagnostics

- AVSBus 1.4/2.0 compliant
- PMBus v1.4.1 compliant
- MTP with up to 31 writes for field programmability
- Black-box registers for fault recording

Package

- 6mm × 6mm, 52-pin QFN
- RoHS compliant and green

Applications

- Server and AI Computing Core Power
- CPU and GPU Core Power
- High-Performance Computing
- Graphics Cards
- Telecom Power Systems

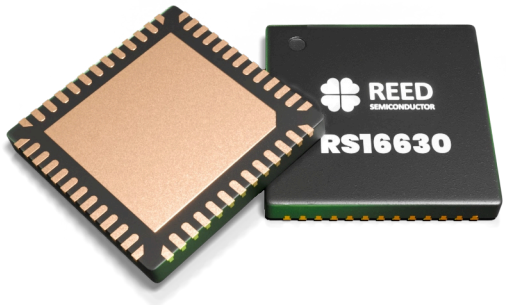
Description

The RS16630 is a high-performance, triple-rail digital multiphase controller supporting up to 6 phases with flexible N + M + O ≤ 6 phase allocation. Designed for high-current computing, server, graphics, and telecom power applications, the device operates from 4.5V to 16V and supports output voltages from 0.2V to 2.7V with ±0.5% output-voltage accuracy.

Native TLVR support, constant-on-time control, programmable DC load-line regulation, and automatic phase add/drop provide fast transient response and efficient operation across changing load conditions. Switching frequencies up to 4MHz enable high-density power conversion, while programmable overshoot and undershoot reduction and thermal phase balancing further optimize transient and thermal performance.

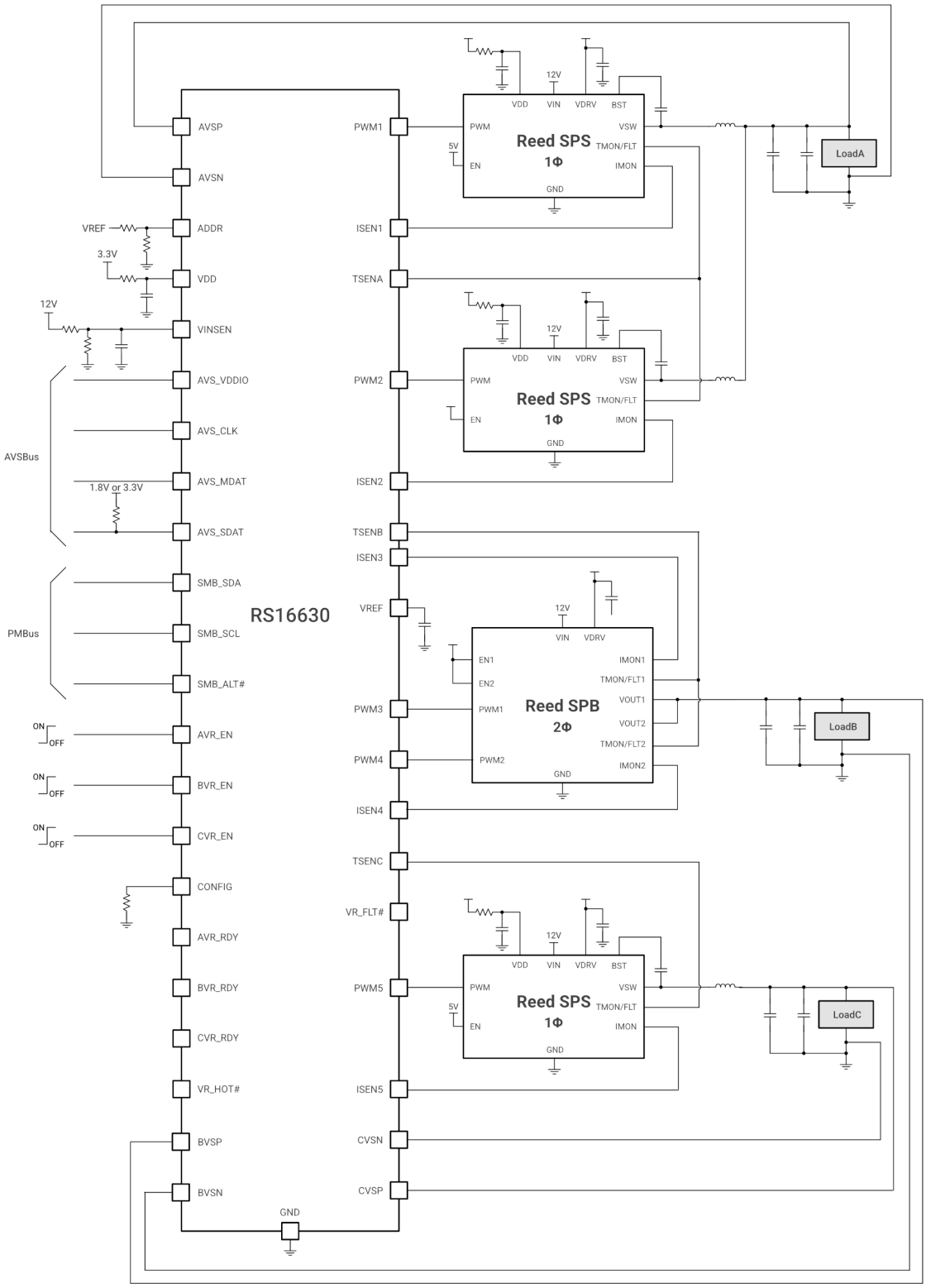
Integrated voltage, current, and temperature telemetry provides real-time system monitoring. The RS16630 supports AVSBus 1.4/2.0 and PMBus v1.4.1, with MTP configuration and black-box fault recording for system configuration and diagnostics. Integrated protection includes UVLO, UVP, OVP, OCP, OTP, cycle-by-cycle per-phase current limiting, and programmable latch-off or auto-retry fault response.

When paired with Reed Smart Power Stages or Smart Power Blocks, the RS16630 provides a flexible, high-density power solution for multiple processor and system rails. The device is offered in a 6mm × 6mm, 52-pin QFN package and operates from −40°C to 125°C.



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Typical Application Schematic (2 + 2 + 1)



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Ordering Information

PART NUMBER	PACKAGE	SIZE	MSL RATING	SHIPPING METHOD	PACKAGE MARKING
RS16630R	QFN-52	6 × 6mm		3000u Tape & Reel	R16630

Top Marking



Line 1

- RS: Prefix of Reed Semiconductor (R is replaced by E for engineering lots)
- YY: Year code
- WW: Week code

Line 2

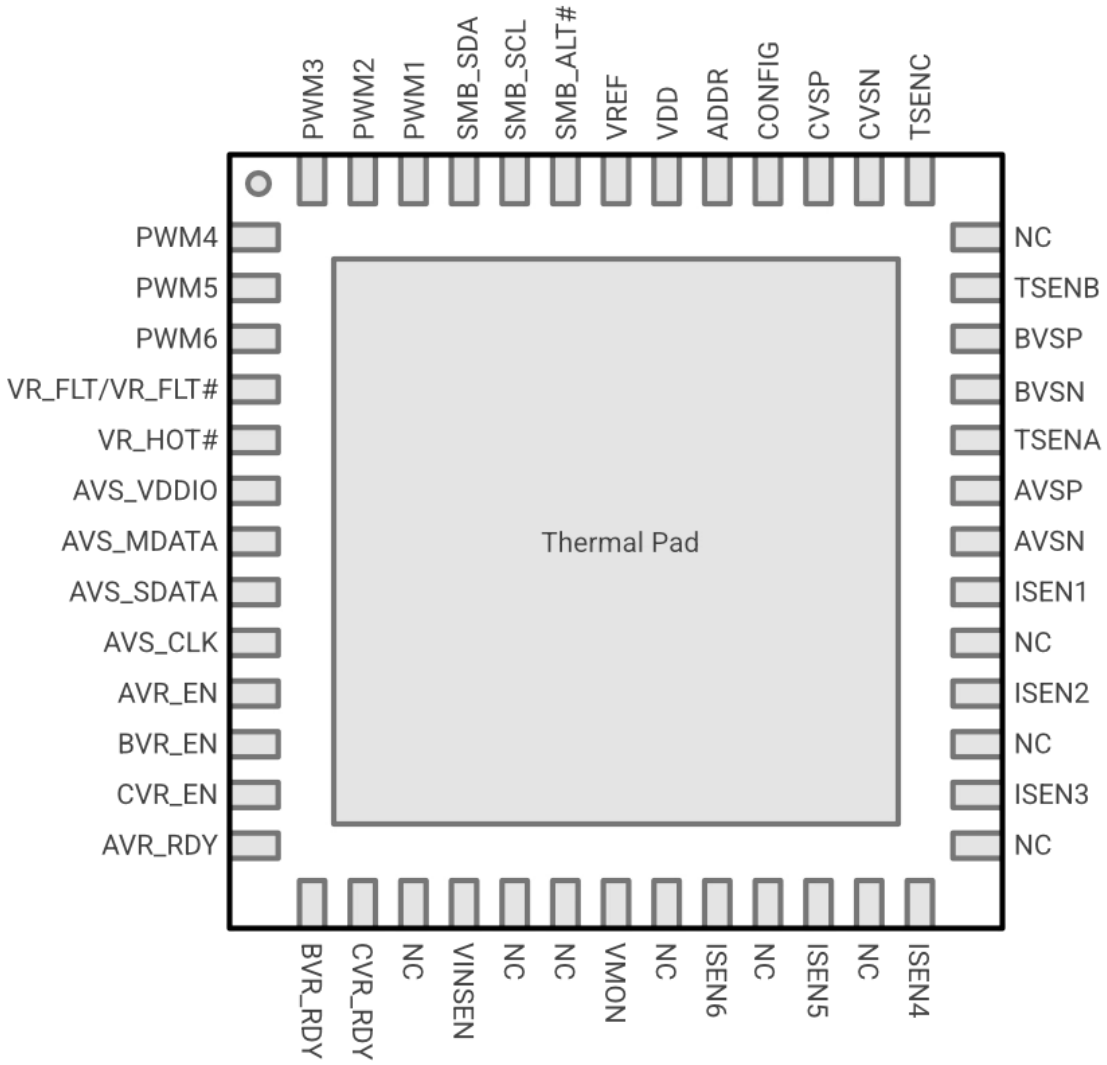
- PPPPP: Truncated part number

Line 3

- LLLLL: Lot code
- S: Assembly site code

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Package Reference



QFN-52 (6 × 6mm)

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Pin Descriptions

PIN	NAME	TYPE	DESCRIPTION
1	PWM4	O	PWM output for Phase 4.
2	PWM5	O	PWM output for Phase 5.
3	PWM6	O	PWM output for Phase 6.
4	VR_FLT/ VR_FLT#	O	Configurable active-high or active-low, open-drain catastrophic-fault output. See Applications section for pull-up requirements.
5	VR_HOT#	O	VR_HOT#: Active-low, open-drain temperature warning output.
6	AVS_VDDIO	P	AVSBus interface supply and I/O reference voltage.
7	AVS_MDATA	I	AVSBus command data input.
8	AVS_SDATA	I/O	AVSBus response data output.
9	AVS_CLK	I	AVSBus clock input.
10	AVR_EN	I	Active-high Rail A enable input.
11	BVR_EN	I	Active-high Rail B enable input.
12	CVR_EN	I	Active-high Rail C enable input.
13	AVR_RDY	O	Active-high, open-drain Power Good output for Rail A.
14	BVR_RDY	O	Active-high, open-drain Power Good output for Rail B.
15	CVR_RDY	O	Active-high, open-drain Power Good output for Rail C.
16	NC	—	No internal connection.
17	VINSEN	I	Power-stage input-voltage sense input.
18	NC	—	No internal connection.
19	NC	—	No internal connection.
20	VMON	I	Power-stage driver-voltage sense input.
21	NC	—	No internal connection.
22	ISNE6	I	Phase 6 current-sense input.
23	NC	—	No internal connection.
24	ISEN5	I	Phase 5 current-sense input.
25	NC	—	No internal connection.
26	ISEN4	I	Phase 4 current-sense input.

PWM outputs (Pins 1–3): 3.3V CMOS tri-state outputs. Low: low-side FET ON; High: high-side FET ON; Tri-state: both FETs OFF. If unused, leave floating.

Type: I = Input, O = Output, I/O = Bidirectional, P = Power, G = Ground, — = No Connect.

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Pin Descriptions

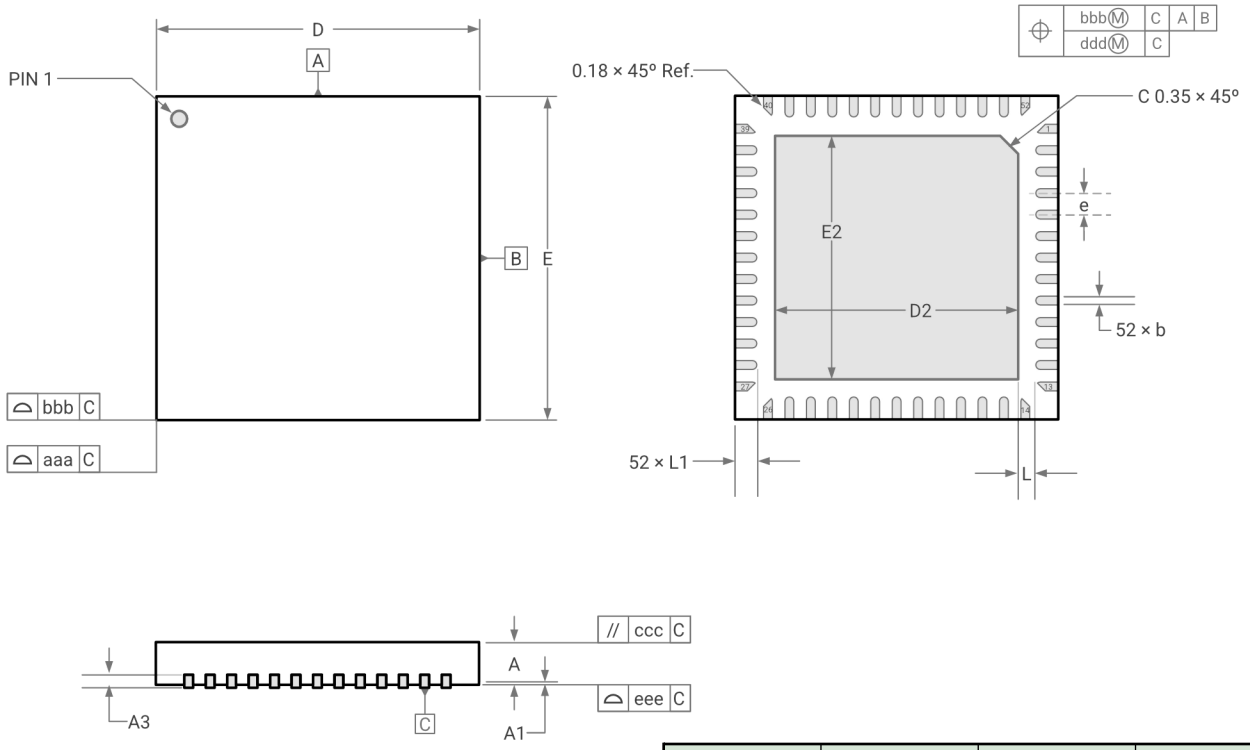
PIN	NAME	TYPE	DESCRIPTION
27	NC	—	No Internal connection
28	ISEN3	I	Phase 3 current-sense input.
29	NC	—	No Internal connection
30	ISEN2	I	Phase 2 current-sense input.
31	NC	—	No Internal connection
32	ISEN1	I	Phase 1 current-sense input.
33	AVSN	I	Rail A negative remote-sense input. Connect to load ground.
34	AVSP	I	Rail A positive remote-sense input. Connect to the output-voltage sense point at the load.
35	TSENA	I	Rail A temperature-sense input.
36	BVSN	I	Rail B negative remote-sense input. Connect to load ground.
37	BVSP	I	Rail B positive remote-sense input. Connect to the output-voltage sense point at the load.
38	TSENB	I	Rail B temperature-sense input.
39	NC	—	No Internal connection
40	TSENC	I	Rail C temperature-sense input.
41	CVSN	I	Rail C negative remote-sense input. Connect to load ground.
42	CVSP	I	Rail C positive remote-sense input. Connect to the output-voltage sense point at the load.
43	CONFIG	I	MTP configuration-select input.
44	ADDR	I	PMBus address-select input.
45	VDD	P	3.3V supply input. Connect a ≥1μF decoupling capacitor to GND.
46	VREF	O	1.5V reference output. Connect a 1μF to 4.7μF decoupling capacitor to GND.
47	SMB_ALT#	O	Active-low, open-drain PMBus ALERT# output.
48	SMB_SCL	I	PMBus serial clock input.
49	SMB_SDA	I/O	PMBus bidirectional serial data.
50	PWM1	O	PWM output for Phase 1.
51	PWM2	O	PWM output for Phase 2.
52	PWM3	O	PWM output for Phase 3.
—	Themal Pad	G	Exposed thermal pad. Connect to the GND plane with multiple thermal vias.

PWM outputs (Pins 50–52): 3.3V CMOS tri-state outputs. Low: low-side FET ON; High: high-side FET ON; Tri-state: both FETs OFF. If unused, leave floating.

Type: I = Input, O = Output, I/O = Bidirectional, P = Power, G = Ground, — = No Connect.

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Package Dimensions



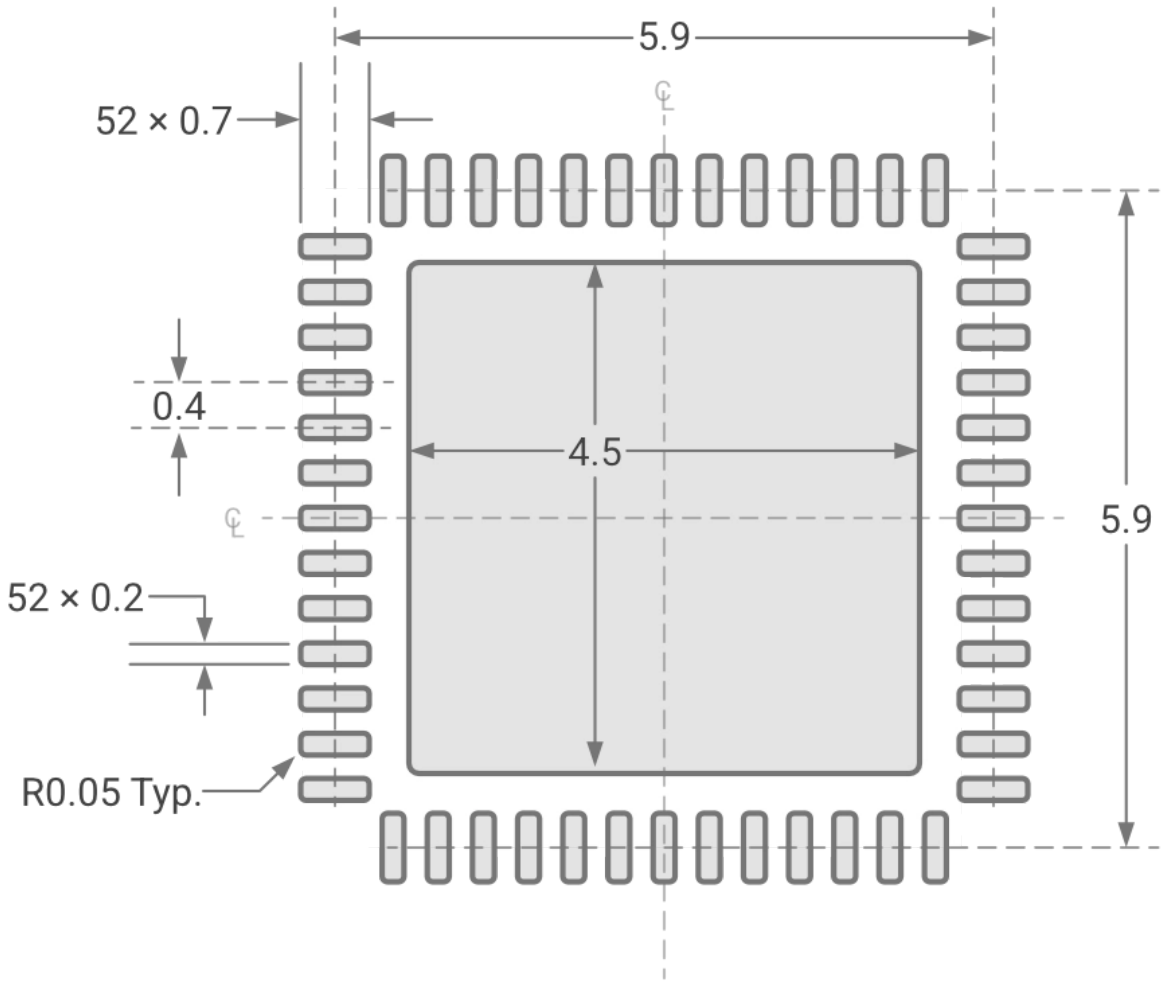
REF	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	—	0.05
A3		0.203 Ref.	
D	5.90	6.00	6.10
E	5.90	6.00	6.10
D2	4.45	4.50	4.55
E2	4.45	4.40	4.55
b	0.15	0.20	0.25
e		0.40 BSC	
L	0.30	0.40	0.50
L1	0.31	0.36	0.41
Geometric Tolerancing			
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	

Notes

1. All dimensions are in millimeters.
2. Drawing per JEDEC MO-220.
3. Drawing is not to scale.

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Recommended Land Pattern

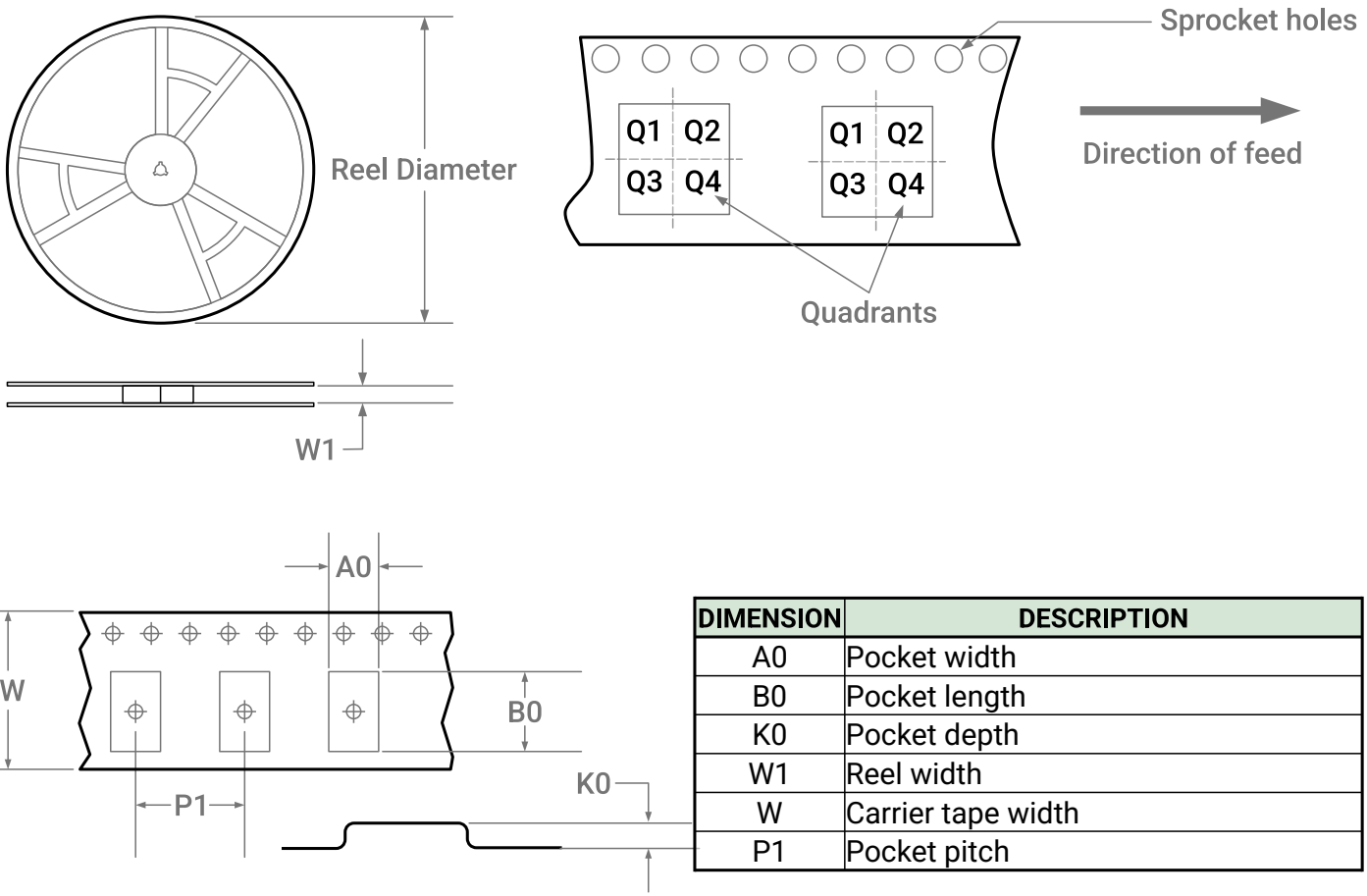


Note:

1. All dimensions are in millimeters.
2. Drawing is not to scale.

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Tape and Reel Information



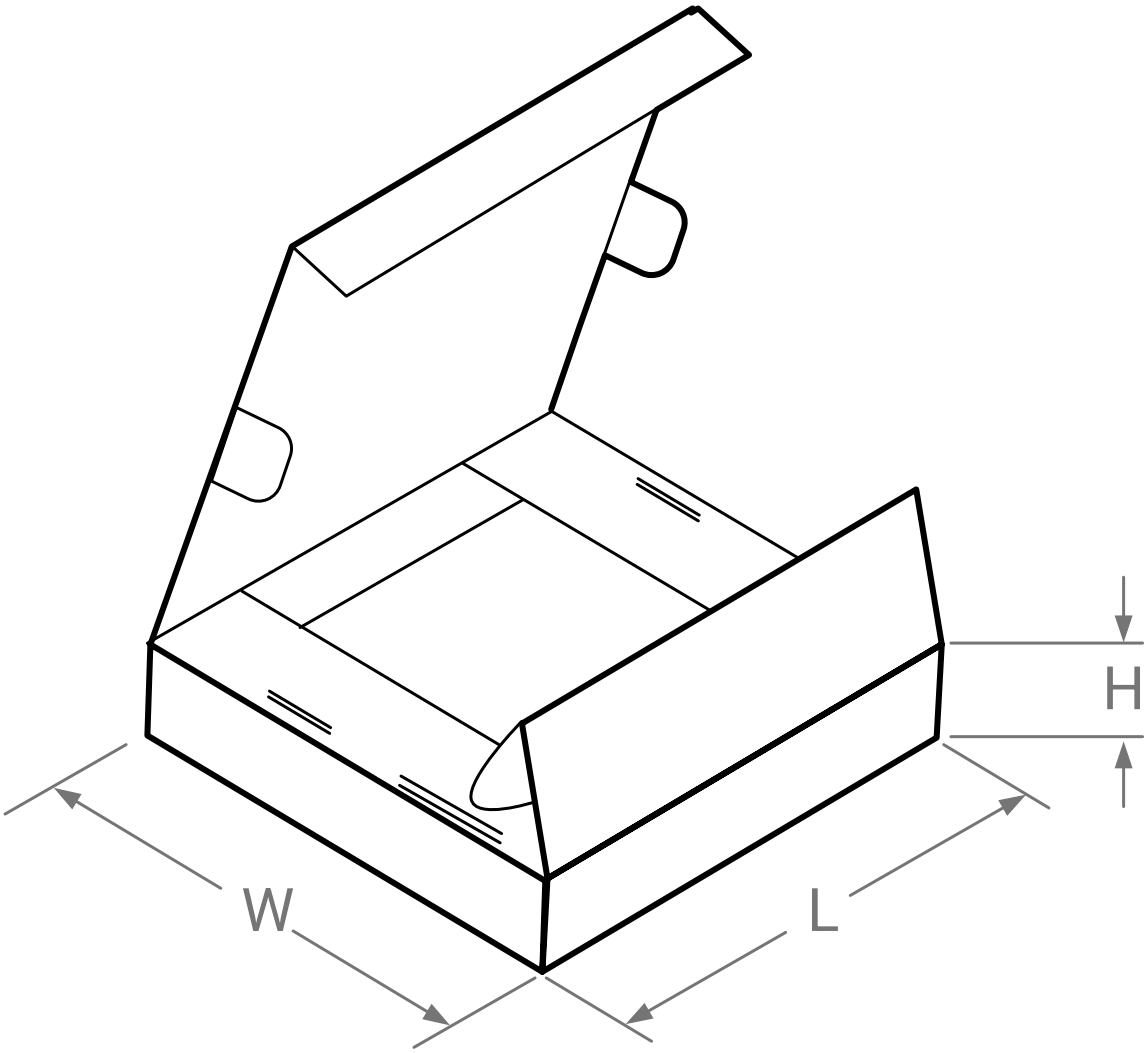
DIMENSION	DESCRIPTION
A0	Pocket width
B0	Pocket length
K0	Pocket depth
W1	Reel width
W	Carrier tape width
P1	Pocket pitch

PACKAGE SIZE	REEL DIAMETER	W1	A0	B0	K0	P1	W	QUADRANT
6 × 6	330	16	6.3	6.3	1.10	12	16	Q2

Note:
1. All dimensions are nominal
2. All dimensions are in millimeters (mm)

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Pizza Box Dimensions



PACKAGE SIZE	UNITS / BOX	LENGTH	WIDTH	HEIGHT
6 × 6	3000	354	337	55

Notes:

1. All measurements are in millimeters;
2. All measurements are nominal.

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