RS19831 Triple-Channel (N+M+O<= 8 Phase) Step-Down Multiphase Controller with SVI3 and PMBus™ Interface

Features

- Native Trans-Inductor Voltage Regulator (TLVR) Support
  - No external passive components required
- Built-in 1kΩ current sense resistor
- Paired with ReedSemi Smart Power Stages or Modules for high density solutions
- Scalability and Flexibility
  - Scalable phase count: (8+0+0) to (5+2+1)
  - Flexible phase order assignment
- Input and Output Range, Accuracy
  - 4.5V to 16V input & 0.2V to 2.7V output
  - 0.5% accurate output with differential sense
- Telemetry
  - 1.5% Input & Output voltage accuracy
  - 1.5% Output current accuracy
  - +/-2°C Temperature accuracy
- Improved Performance
  - Improved efficiency: Programmable Auto phase add/drop thresholds for optimization
  - Programmable Over-shoot & Under-shoot Reduction thresholds for better transient
  - Thermal Balance Management
- Protection Capability
  - Programmable Fault Response: Latch & Hiccup
  - UVLO, UVP, OVP, OCP, OTP
  - Cycle by cycle per-phase current limit
- Output BOM, Platform Area and Cost Reduction
  - Up to 4MHz switching frequency & Constant On Time control with fast transient for smaller & low-cost external passives
  - Programmable DC load line helps reduce the overshoot and the external capacitors
- Ease-of-use, Interfaces and Debug Features
  - Internal compensation
  - AMD SVI3 revision 3.0 Compliant
  - PMBus™ v1.4.1 Compliant
  - Built in Multiple time Programmability (MTP) with up to 31 writes for field programmability
  - Black box registers for fault record
- RoHS Compliant and Green
- 6 mm × 6 mm, 52-Pin, QFN Package

Applications

- Server and Telecom Voltage Regulators
- Graphic Card Core Regulators
- Power Module

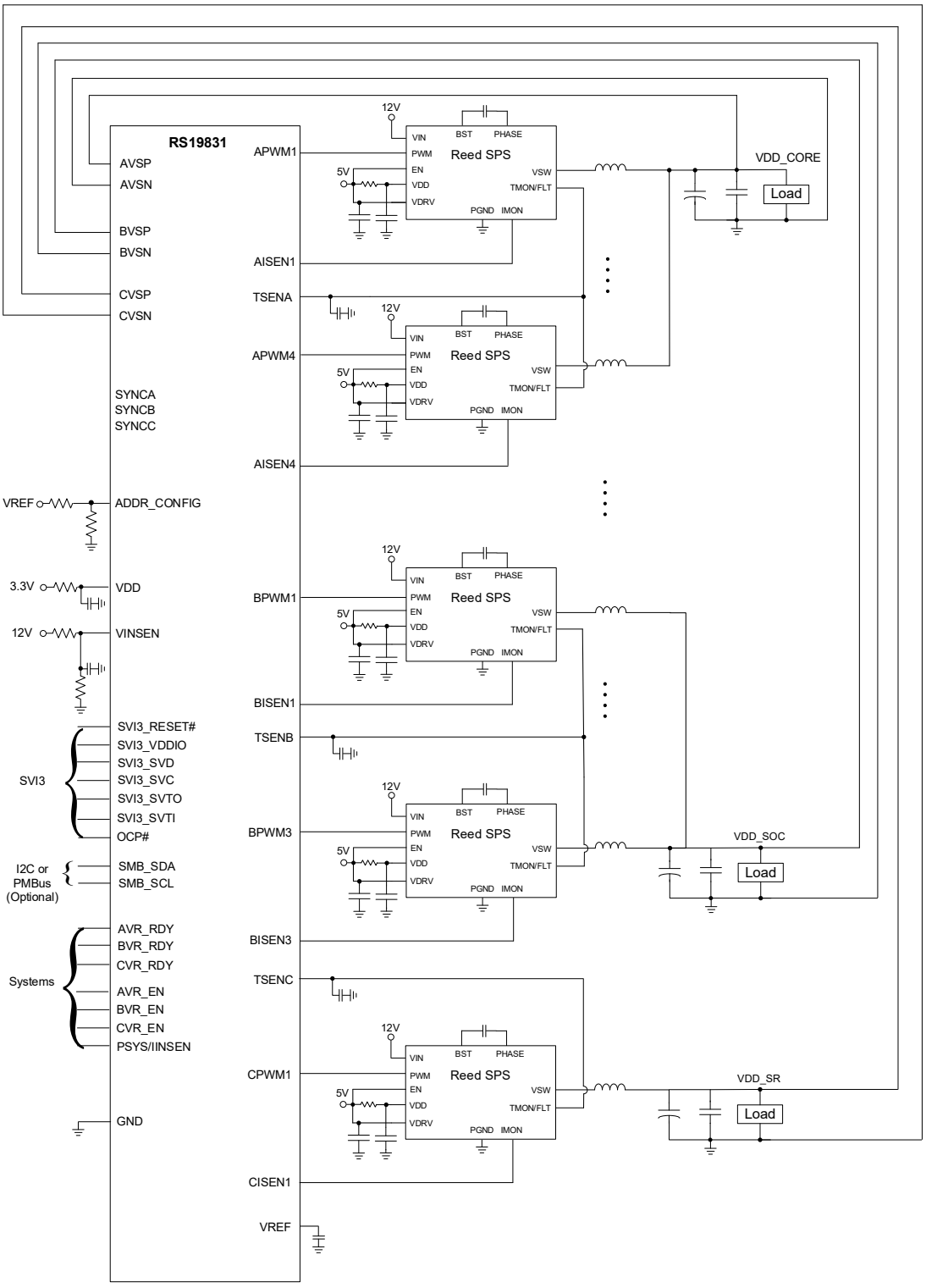
Description

RS19831 is a SVI3 compliant dual output multiphase buck controller with built-in MTP & PMBus™ interface. It is fully compatible with Reed Semiconductor's smart power stage. Advanced control features such as programmable DC load line, undershoot & overshoot reduction provide fast transient response hence needing low output capacitance. The device also provides auto phase add/drop with phase current balancing for efficiency improvement across loads. It supports fast dynamic voltage transitions with programable slew rates. All programmable parameters can be configured by the PMBus interface and can be stored in devices as default values. The MTP gives an added advantage of optimizing the device performance in the field.

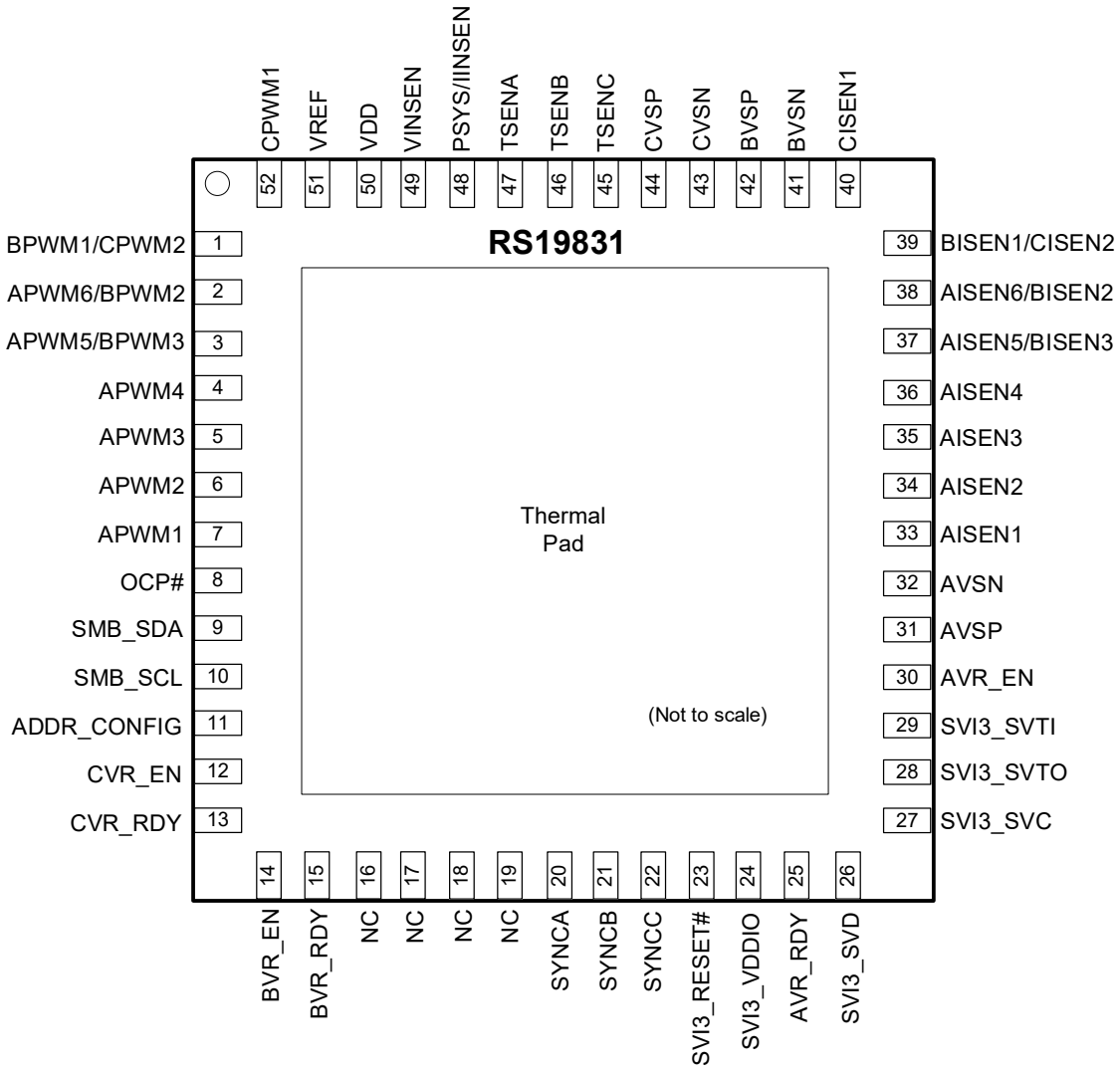
RS19831 is offered in a 52-pin QFN package and is rated to operate from -40°C to 125°C

Typical Application Circuit

Application Example (4+2+1)



Pin Description List



PIN		I/O	Type	DESCRIPTION	
No.	NAME				
1	BPWM1/CPWM2	O	3.3V CMOS	PWM signal for Phase 1 of Rail B/ Phase 2 of Rail C	**Tri-state logic level:** 0V: Low Side FET ON 3.3V: High Side FET ON Tri-state (tied to VREF): Both FETs OFF If unused, leave them floating
2	APWM6/BPWM2			PWM signal for Phase 6 of Rail A/ Phase 2 of Rail B	
3	APWM5/BPWM3			PWM signal for Phase 5 of Rail A/ Phase 3 of Rail B	
4	APWM4			PWM signal for Phase 4 of Rail A	
5	APWM3			PWM signal for Phase 3 of Rail A	
6	APWM2			PWM signal for Phase 2 of Rail A	
7	APWM1			PWM signal for Phase 1 of Rail A	
8	OCP#/	O	Open Drain	Active low output, asserted when current is greater than SVI3 OCP_THRESH or SVI3 OCP_WARN_THRESH	
9	SMB_SDA	I/O	Open Drain	PMBus bi-directional serial data signal	
10	SMB_SCL	I	Open Drain	PMBus serial clock signal	
11	ADDR_CONFIG	I	CMOS	Combined ADDR and CONFIG pin, this pin works as ADDR during VDD ramping up when the top and bottom resistors are installed, as CONFIG when the bottom resistor is installed only.	
12	CVR_EN	I	CMOS	This pin used as Active High Enable for the Rail C.	
13	CVR_RDY	O	Open Drain	Active high, Power Good output asserts when the output voltage of Rail C is in regulation.	
14	BVR_EN	I	CMOS	This pin used as Active High Enable for the Rail B.	
15	BVR_RDY	O	Open Drain	Active high, Power Good output asserts when the output voltage of Rail B is in regulation.	
16	NC			Not connected	
17	NC			Not connected	
18	NC			Not connected	
19	NC			Not connected	
20	SYNCA	O	CMOS	Synchronization control pin of Rail A. Tie to all the SYNC pin of Smart Power Stage for power saving. PSI0 – SYNCA = 3.3V PSI1/2/3 – SYNCA = 0V PSI6 – SYNCA = 1.5V	
21	SYNCB	O	CMOS	Synchronization control pin of Rail A. Tie to all the SYNC pin of Smart Power Stage for power saving. PSI0 – SYNCA = 3.3V PSI1/2/3 – SYNCA = 0V PSI6 – SYNCA = 1.5V	

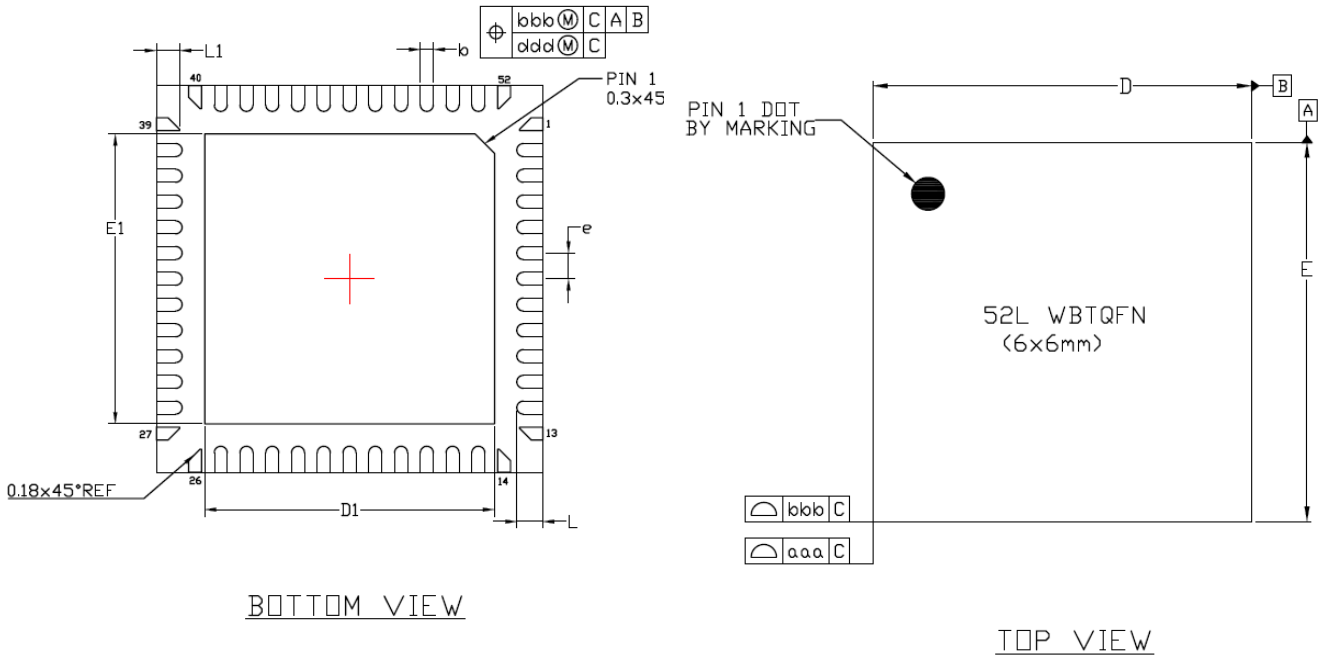
22	SYNCC	O	CMOS	Synchronization control pin of Rail A. Tie to all the SYNC pin of Smart Power Stage for power saving. PSI0 – SYNCA = 3.3V PSI1/2/3 – SYNCA = 0V PSI6 – SYNCA = 1.5V	
23	SVI3_RESET#	I	CMOS	Active low signal causing all SVI3 state machines and SVI3-defined registers to reset to default states.	
24	SVI3_VDDIO	I	Power	VDDIO powers and serves as the reference the SVI3 interface pins: SVD, SVTI and SVTO, needs a decoupling cap of ≥1uF to GND.	
25	AVR_RDY	O	Open Drain	Active high, Power Good output asserts when the output voltage of Rail A is in regulation.	
26	SVI3_SVD	I	CMOS	Serial VID Data is a push-pull signal which transmits commands from the master to the slaves.	
27	SVI3_SVC	I	CMOS	Serial VID Clock is a push-pull signal which acts as a clock for SVD, SVTI and SVTO.	
28	SVI3_SVTO	O	CMOS	Serial VID Telemetry Output is a push-pull output driven by each slave. It carries telemetry and acknowledge packets.	
29	SVI3_SVTI	I	CMOS	Serial VID Telemetry Input is driven by the next-furthest slave (from the master) on the telemetry daisy-chain. It carries telemetry and acknowledge packets.	
30	AVR_EN	I	CMOS	This pin used as Active High Enable for the Rail A.	
31	AVSP	I	Analog	Rail A output remote voltage sense at the load point	
32	AVSN	I	Analog	Rail A GND remote voltage sense at the load point	
33	AISEN1	I	Analog	Current Sense of Rail A Phase 1	If unused, leave them floating
34	AISEN2			Current Sense of Rail A Phase 2	
35	AISEN3			Current Sense of Rail A Phase 3	
36	AISEN4			Current Sense of Rail A Phase 4	
37	AISEN5/BISEN3			Current Sense of Rail A Phase 5/ Rail B Phase 3	
38	AISEN6/BISEN2			Current Sense of Rail A Phase 6/ Rail B Phase 2	
39	BISEN1/CISEN2			Current Sense of Rail B Phase 1/ Rail C Phase 2	
40	CISEN1			Current Sense of Rail C Phase 1	
41	BVSN	I	Analog	Rail B GND remote voltage sense at the load point	
42	BVSP	I	Analog	Rail B output remote voltage sense at the load point	
43	CVSN	I	Analog	Rail C GND remote voltage sense at the load point	
44	CVSP	I	Analog	Rail C output remote voltage sense at the load point	
45	TSENC	I	Analog	Temperature Sense input from all the phases of Rail C	
46	TSENB	I	Analog	Temperature Sense input from all the phases of Rail B	
47	TSENA	I	Analog	Temperature Sense input from all the phases of Rail A	
48	PSYS/IINSEN	I	Analog	This is a multi-function pin, can be configured as PSYS or IINSEN through MTP registers *PSYS – input power per system, pull a resistor to GND on this pin and not exceeding VREF (1.5V)* *IINSEN – input current sense, pull a resistor to GND on this pin*	

				and not exceeding VREF (1.5V)	
49	VINSEN	I	Analog	To sense input voltage of power stages with a resistive voltage divider (1/6), needs a decoupling cap of 0.1uF to GND	
50	VDD	I	Power	3.3V supply voltage input. Needs a decoupling cap of ≥1uF to GND.	
51	VREF	O	Power	1.5V reference voltage output. Needs a decoupling cap of 1uF to GND	
52	CPWM1	O	3.3V CMOS	PWM signal for Phase 1 of Rail C	**logic level:** 0V: Low Side FET ON 3.3V: High Side FET ON Tri-state (tied to VREF): Both FETs OFF If unused, leave them floating
*	Thermal Pad	I	Ground	Ground pad, tie to GND plane with vias.	

Ordering Information

Part Number	Package	Shipping Method	Package Marking
RS19831R	QFN-52	3ku Tape & Reel	R19831

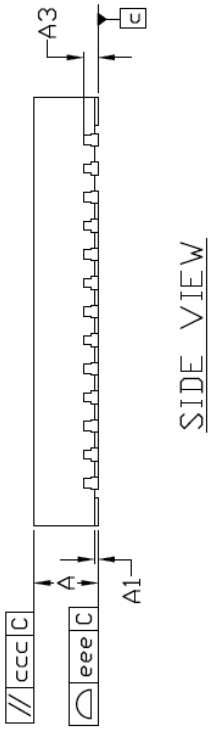
Package information



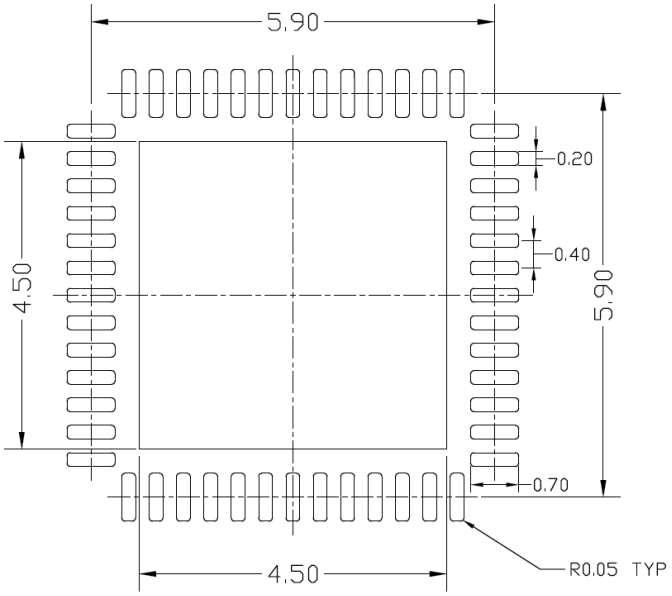
Notes

1. All DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER JEDEC MO-220.
3. DRAWING IS NOT TO SCALE.

Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	---	---	0.05
A3	0.203 Ref.		
D	5.90	6.00	6.10
E	5.90	6.00	6.10
D1	4.45	4.50	4.55
E1	4.45	4.50	4.55
b	0.15	0.20	0.25
e	0.40BSC		
L	0.35	0.40	0.45
L1	0.31	0.36	0.41
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		



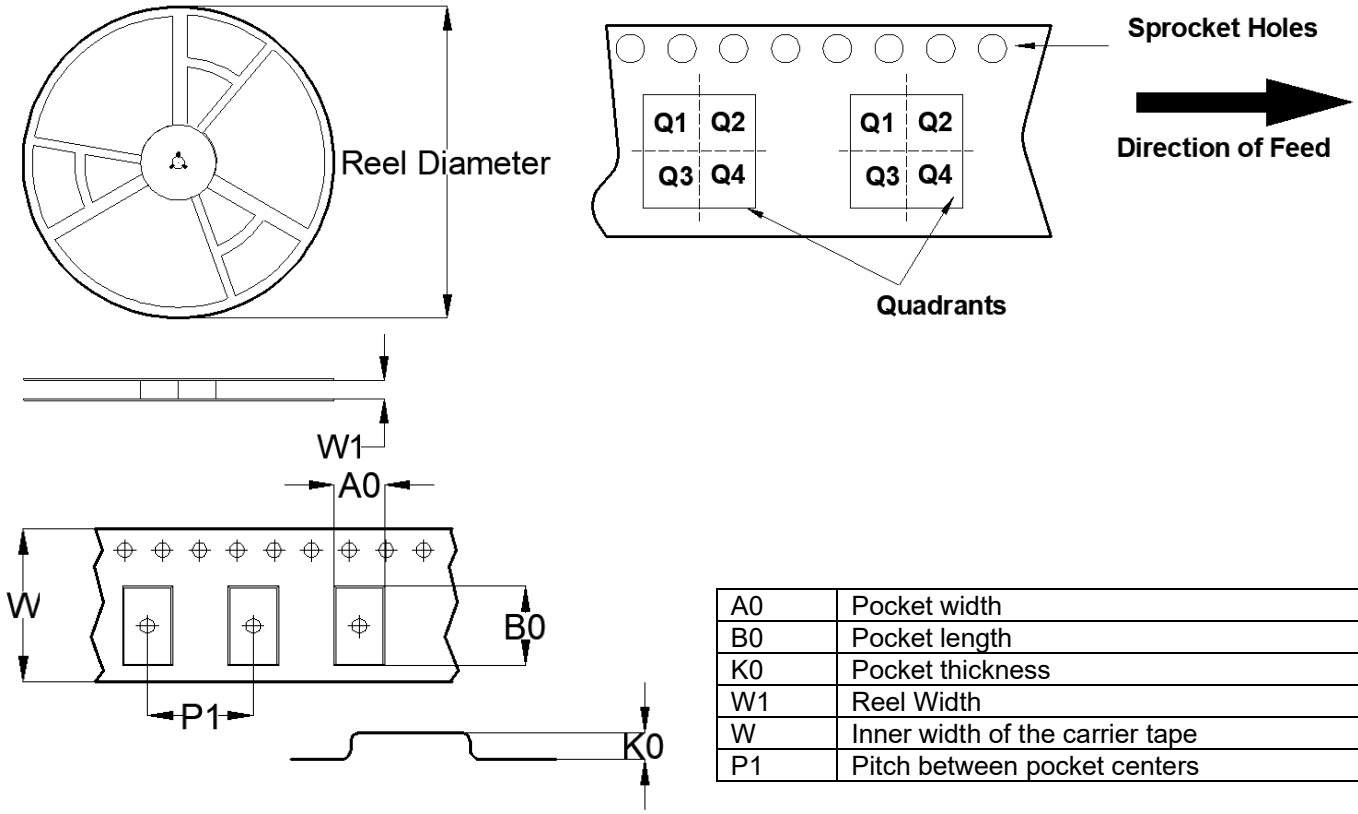
Recommended Land Pattern



NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

Tape and Reel Information

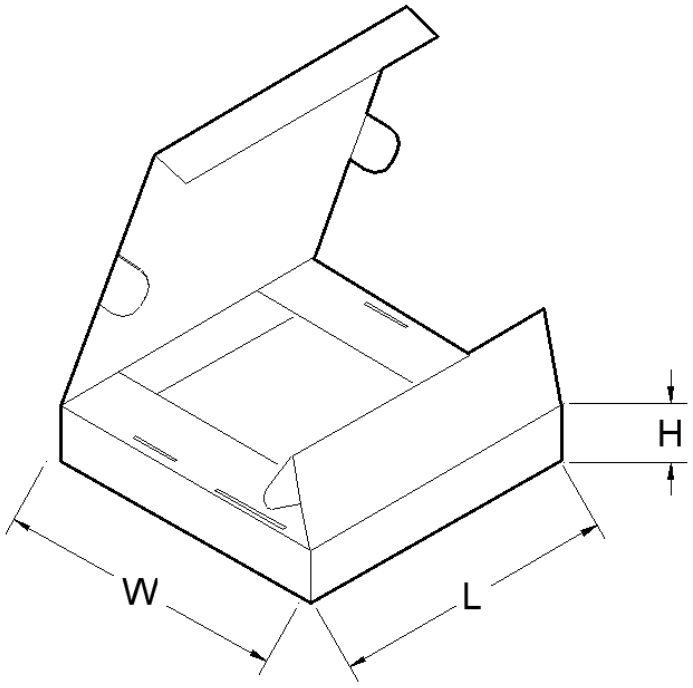


A0	Pocket width
B0	Pocket length
K0	Pocket thickness
W1	Reel Width
W	Inner width of the carrier tape
P1	Pitch between pocket centers

PKG type(mm)	Reel Diameter(mm)	Reel Width W1(mm)	A0(mm)	B0(mm)	K0(mm)	P1(mm)	W(mm)	Quad
6x6	330	16	6.3	6.3	1.1	12	16	Q2

*All the data is nominal

Pizza Box Dimension



PKG type(mm)	Units/box	Length(mm)	Width(mm)	Height(mm)
6x6	3000	354	337	55

*All the data is nominal