
RS18G30 Triple-Channel (N+M+O≤ 16 Phase) Step-Down Multiphase Controller with SVID/SVI3/AVSBus and PMBus™ Interface

Features

- Native Trans-Inductor Voltage Regulator (TLVR) Support
 - No external passive components required
- Built-in 1kΩ current sense resistor
- Paired with ReedSemi Smart Power Stages or Modules for high density solutions
- Scalability and Flexibility
 - Scalable phase count: (16+0+0) to (8+4+4)
 - Flexible phase order assignment
- Input and Output Range, Accuracy
 - 4.5V to 16V input & 0.2V to 2.7V output
 - 0.5% accurate output with differential sense
- Telemetry
 - 1.5% Input & Output voltage accuracy
 - 1.5% Output current accuracy
 - +/-2°C Temperature accuracy
- Improved Performance
 - Improved efficiency: Programmable Auto phase add/drop thresholds for optimization
 - Programmable Over-shoot & Under-shoot Reduction thresholds for better transient
 - Thermal Balance Management
- Protection Capability
 - Programmable Fault Response: Latch & Hiccup
 - UVLO, UVP, OVP, OCP, OTP
 - Cycle by cycle per-phase current limit
- Output BOM, Platform Area and Cost Reduction
 - Up to 4MHz switching frequency & Constant On Time control with fast transient for smaller & low-cost external passives
 - Programmable DC load line helps reduce the overshoot and the external capacitors
- Ease-of-use, Interfaces and Debug Features
 - Internal compensation
 - PMBus™ v1.4.1/SVID/AVSBus 1.4/2.0/SVI3 2.0/3.0 Compliant
 - Built in Multiple time Programmability (MTP) with up to 31 writes for field programmability
 - Black box registers for fault record
- RoHS Compliant and Green
- 7 mm × 7 mm, 60-Pin, QFN Package

Applications

- Server and Telecom Voltage Regulators
- Graphic Card Core Regulators
- Power Module

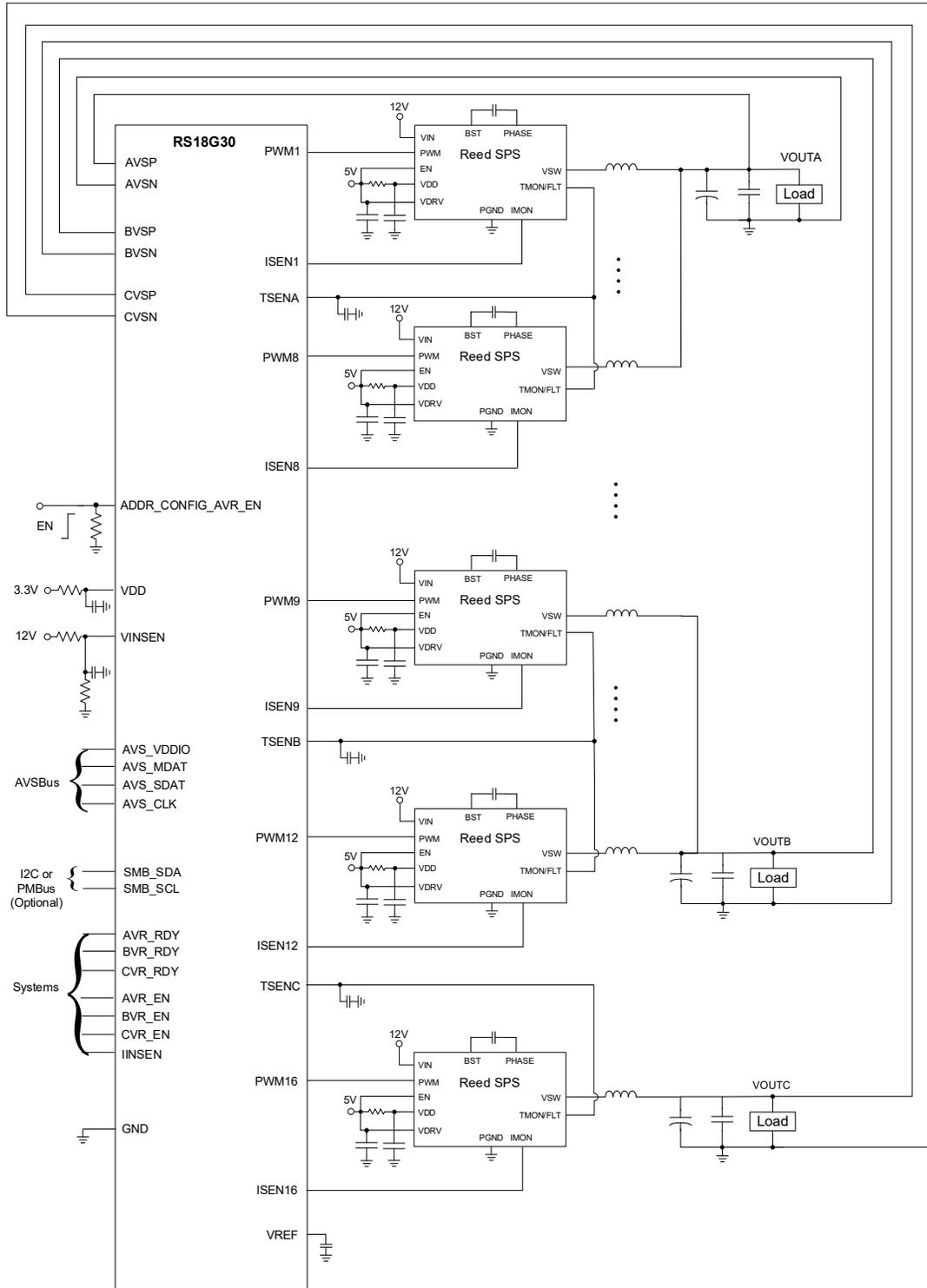
Description

RS18G30 is a SVID/SVI3/AVSBus compliant triple output multiphase buck controller with built-in MTP & PMBus™ interface. It is fully compatible with Reed Semiconductor's smart power stage. Advanced control features such as programmable DC load line, undershoot & overshoot reduction provide fast transient response hence needing low output capacitance. The device also provides auto phase add/drop with phase current balancing for efficiency improvement across loads. It supports fast dynamic voltage transitions with programmable slew rates. All programmable parameters can be configured by the PMBus interface and can be stored in devices as default values. The MTP gives an added advantage of optimizing the device performance in the field.

RS18G30 is offered in a 60-pin QFN package and is rated to operate from -40°C to 125°C

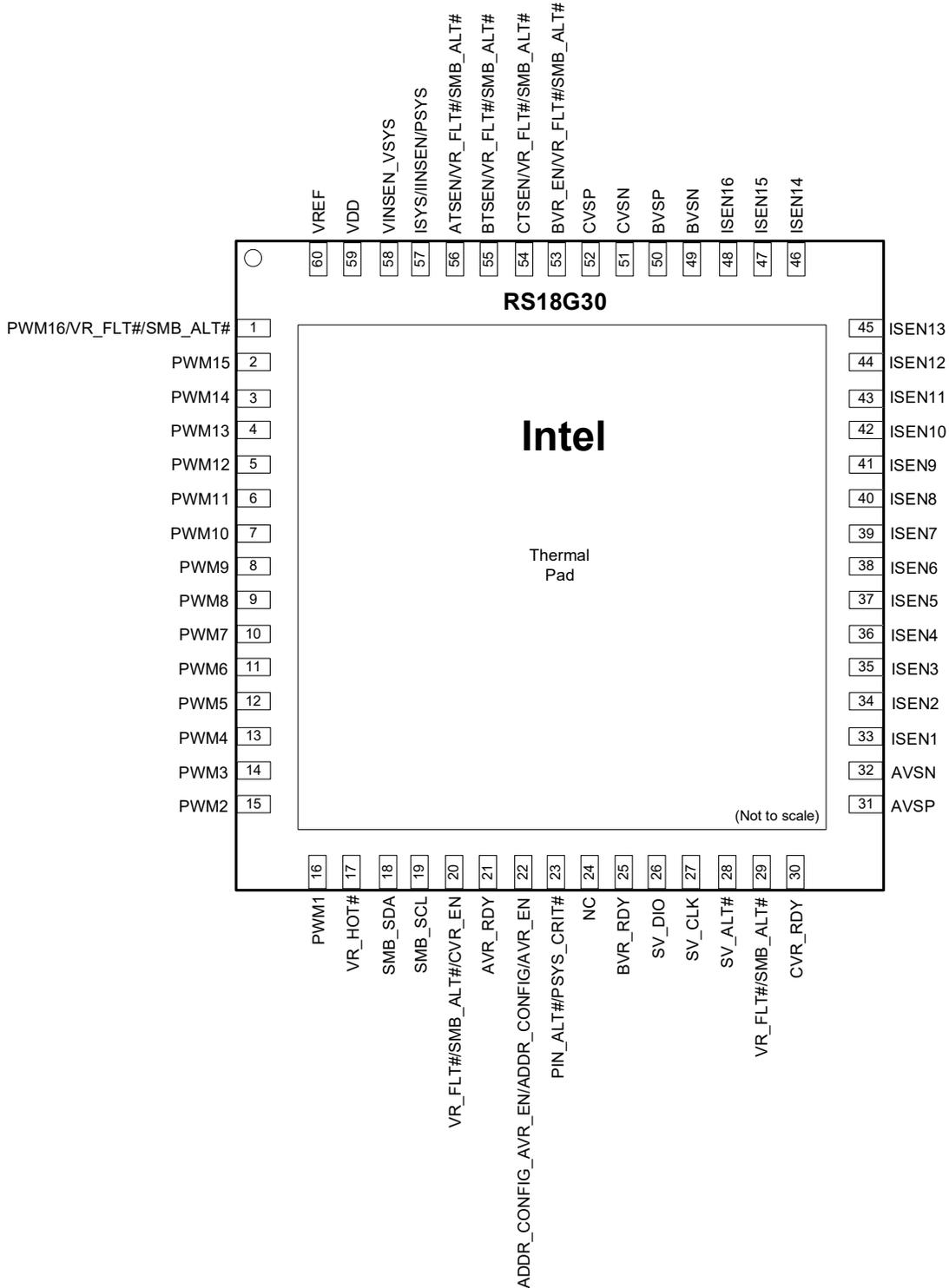
Typical Application Circuit

Application Example (8+4+1)



Pin Description List

The controller supports either SVID, SVI3 or AVSBus by set TOP_CHIP_CFG_52[3:0].
When TOP_CHIP_CFG_52[3:0]=000b(VR13) or 001b(VR14), the pinout becomes as follows:

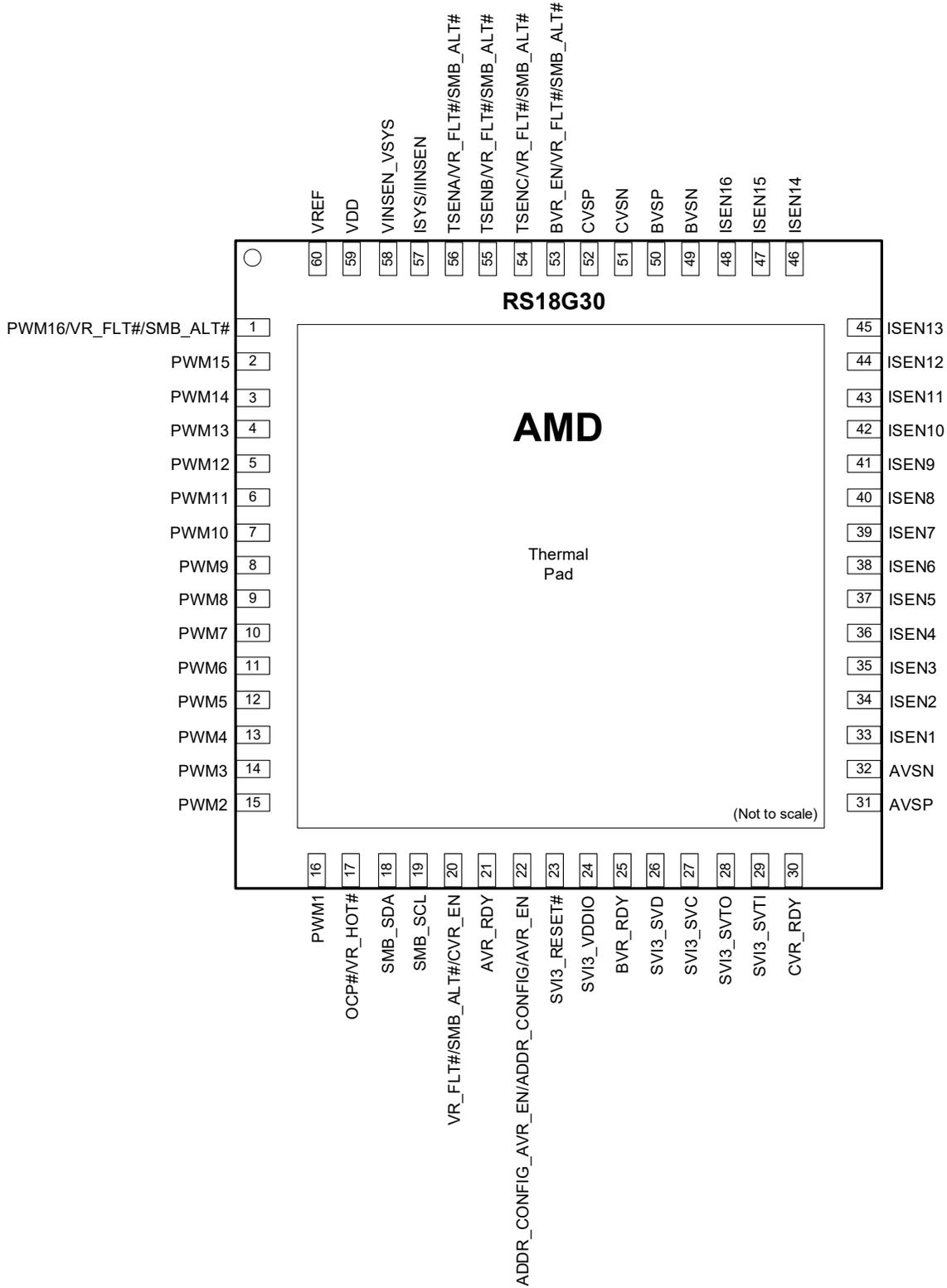


Intel				
PIN		I/O	Type	DESCRIPTION
No.	NAME			
1	PWM16/VR_FLT#/SMB_ALT#	O	3.3V CMOS / Open Drain	PWM16 – PWM signal for Phase 16 VR_FLT# – Active low catastrophic fault pin indicator, controller stops regulating when this pin is pulled low. SMB_ALT# – PMBus active low ALERT# signal.
2	PWM15		PWM signal for Phase 15	
3	PWM14		PWM signal for Phase 14	
4	PWM13		PWM signal for Phase 13	
5	PWM12		PWM signal for Phase 12	
6	PWM11		PWM signal for Phase 11	
7	PWM10		PWM signal for Phase 10	
8	PWM9		PWM signal for Phase 9	
9	PWM8		PWM signal for Phase 8	
10	PWM7		PWM signal for Phase 7	
11	PWM6		PWM signal for Phase 6	
12	PWM5		PWM signal for Phase 5	
13	PWM4		PWM signal for Phase 4	
14	PWM3		PWM signal for Phase 3	
15	PWM2		PWM signal for Phase 2	
16	PWM1		PWM signal for Phase 1	
17	VR_HOT#	O	Open Drain	Active low smart power stage temperature indicator. VRHOT# is asserted at the temperature configured by (51h)OT_WARN_LIMIT.
18	SMB_SDA	I/O	Open Drain	PMBus bi-directional serial data signal.
19	SMB_SCL	I	Open Drain	PMBus serial clock signal.
20	VR_FLT#/SMB_ALT#/CVR_EN	I/O	Open Drain/C MOS	VR_FLT# – Active low catastrophic fault pin indicator, controller stops regulating when this pin is pulled low. SMB_ALT# – PMBus active low ALERT# signal. CVR_EN – This pin used as Active High Enable for the Rail C.
21	AVR_RDY	O	Open Drain	Active high, Power Good output asserts when the output voltage of Rail A is in regulation.
22	ADDR_CONFIG_AVR_EN/ADDR_CONFIG/AVR_EN	I	Analog/CMOS	ADDR_CONFIG_AVR_EN – Combined ADDR_CONFIG and AVR_EN pin, this pin works as ADDR_CONFIG during VDD ramping up, after address is latched, works as AVR_EN. ADDR_CONFIG – Combined ADDR and CONFIG pin, this pin works as ADDR during VDD ramping up when the top and bottom resistors are installed, as CONFIG when the bottom resistor is installed only. AVR_EN – This pin used as Active High Enable for the Rail A.
23	PIN_ALT#/PSYS_CRIT#	O	Open Drain	This is a multi-function pin, can be configured as PIN_ALT# or PSYS_CRIT# through MTP registers (IO_CFG_2_67h)

				Active low alert pin to assert if the input power per rail or input power per system exceeds user defined threshold. Pull-up to an external voltage through a resistor.
24	NC			Not connected
25	BVR_RDY	O	Open Drain	Active high, Power Good output asserts when the output voltage of Rail B is in regulation.
26	SV_DIO	I/ O	Open Drain	SVID bi-directional data interface. Pull-up to an external voltage (typical 1.0V) through a resistor.
27	SV_CLK	I	CMOS	SVID clock interface. Pull-up to an external voltage (typical 1.0V) through a resistor.
28	SV_ALT#	O	Open Drain	SVID active low ALERT# signal. This output is asserted to indicate the status of the VR has changed. Pull-up to an external voltage (typical 1.0V) through a resistor.
29	VR_FLT#/SMB_ALT#	O	Open Drain	VR_FLT# – Active low catastrophic fault pin indicator, controller stops regulating when this pin is pulled low. SMB_ALT# – PMBus active low ALERT# signal.
30	CVR_RDY	O	Open Drain	Active high, Power Good output asserts when the output voltage of Rail C is in regulation.
31	AVSP	I	Analog	Rail A output remote voltage sense at the load point
32	AVSN	I	Analog	Rail A GND remote voltage sense at the load point
33	ISEN1	I	Analog	Current Sense of Phase 1
34	ISEN2			Current Sense of Phase 2
35	ISEN3			Current Sense of Phase 3
36	ISEN4			Current Sense of Phase 4
37	ISEN5			Current Sense of Phase 5
38	ISEN6			Current Sense of Phase 6
39	ISEN7			Current Sense of Phase 7
40	ISEN8			Current Sense of Phase 8
41	ISEN9			Current Sense of Phase 9
42	ISEN10			Current Sense of Phase 10
43	ISEN11			Current Sense of Phase 11
44	ISEN12			Current Sense of Phase 12
45	ISEN13			Current Sense of Phase 13
46	ISEN14			Current Sense of Phase 14
47	ISEN15			Current Sense of Phase 15
48	ISEN16			Current Sense of Phase 16
49	BVSN	I	Analog	Rail B GND remote voltage sense at the load point
50	BVSP	I	Analog	Rail B output remote voltage sense at the load point
51	CVSN	I	Analog	Rail C GND remote voltage sense at the load point
52	CVSP	I	Analog	Rail C output remote voltage sense at the load point
53	BVR_EN/VR_FLT#/SMB_ALT#	I/ O	Open Drain/C	BVR_EN – This pin used as Active High Enable for the Rail B. VR_FLT# – Active low catastrophic fault pin indicator, controller

			MOS	stops regulating when this pin is pulled low. SMB_ALT# – PMBus active low ALERT# signal.
54	TSENC/VR_FLT#/SMB_ALT#	I/O	Open Drain/C MOS	TSENC – Temperature Sense input from all the phases of Rail C VR_FLT# – Active low catastrophic fault pin indicator, controller stops regulating when this pin is pulled low. SMB_ALT# – PMBus active low ALERT# signal.
55	TSENB/VR_FLT#/SMB_ALT#	I/O	Open Drain/C MOS	TSENB – Temperature Sense input from all the phases of Rail B VR_FLT# – Active low catastrophic fault pin indicator, controller stops regulating when this pin is pulled low. SMB_ALT# – PMBus active low ALERT# signal.
56	TSENA/VR_FLT#/SMB_ALT#	I/O	Open Drain/C MOS	TSENA – Temperature Sense input from all the phases of Rail A VR_FLT# – Active low catastrophic fault pin indicator, controller stops regulating when this pin is pulled low. SMB_ALT# – PMBus active low ALERT# signal.
57	ISYS/IINSEN/PSYS	I	Analog	ISYS/IINSEN – input current sense, pull a resistor to GND on this pin and not exceeding VREF (1.5V) PSYS – input power per system, pull a resistor to GND on this pin and not exceeding VREF (1.5V)
58	VSYS/VINSEN	I	Analog	To sense input voltage of power stages with a resistive voltage divider (1/6), needs a decoupling cap of 0.1uF to GND. This pin also represents the VSYS.
59	VDD	I	Power	3.3V supply voltage input. Needs a decoupling cap of $\geq 1\mu\text{F}$ to GND
60	VREF	O	Power	1.5V reference voltage output. Needs a decoupling cap of $1\mu\text{F}$ to GND, but not greater than $4.7\mu\text{F}$
*	Thermal Pad	I	Ground	Ground pad, tie to GND plane with vias.

When TOP_CHIP_CFG_52[3:0]=011b(SVI3), the pinout becomes as follows:

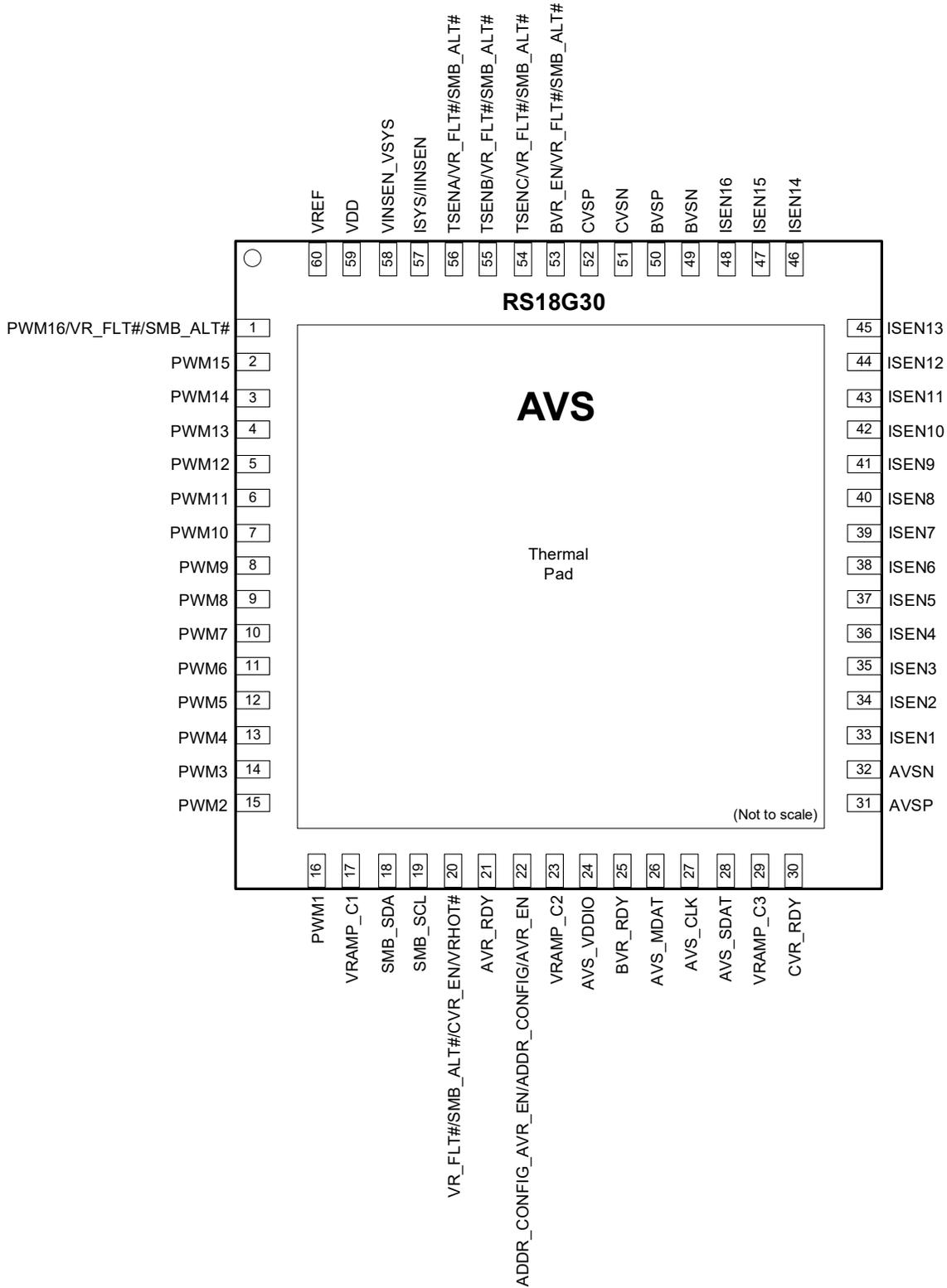


AMD				
PIN		I/ O	Type	DESCRIPTION
No.	NAME			
1	PWM16/VR_FLT#/SMB_ALT#	O	3.3V CMOS / Open Drain	PWM16 – PWM signal for Phase 16 VR_FLT# – Active low catastrophic fault pin indicator, controller stops regulating when this pin is pulled low. SMB_ALT# – PMBus active low ALERT# signal.
2	PWM15		PWM signal for Phase 15	
3	PWM14		PWM signal for Phase 14	
4	PWM13		PWM signal for Phase 13	
5	PWM12		PWM signal for Phase 12	
6	PWM11		PWM signal for Phase 11	
7	PWM10		PWM signal for Phase 10	
8	PWM9		PWM signal for Phase 9	
9	PWM8		PWM signal for Phase 8	
10	PWM7		PWM signal for Phase 7	
11	PWM6		PWM signal for Phase 6	
12	PWM5		PWM signal for Phase 5	
13	PWM4		PWM signal for Phase 4	
14	PWM3		PWM signal for Phase 3	
15	PWM2		PWM signal for Phase 2	
16	PWM1		PWM signal for Phase 1	
17	OCP#/VR_HOT#	O	Open Drain	OCP# – Active low output, asserted when current is greater than SVI3 OCP_THRESH or SVI3 OCP_WARN_THRESH VR_HOT – Active low smart power stage temperature indicator. VRHOT# is asserted at the temperature configured by (51h)OT_WARN_LIMIT.
18	SMB_SDA	I/O	Open Drain	PMBus bi-directional serial data signal.
19	SMB_SCL	I	Open Drain	PMBus serial clock signal.
20	VR_FLT#/SMB_ALT#/CVR_EN	I/O	Open Drain/C MOS	VR_FLT# – Active low catastrophic fault pin indicator, controller stops regulating when this pin is pulled low. SMB_ALT# – PMBus active low ALERT# signal. CVR_EN – This pin used as Active High Enable for the Rail C.
21	AVR_RDY	O	Open Drain	Active high, Power Good output asserts when the output voltage of Rail A is in regulation.
22	ADDR_CONFIG_AVR_EN/ADDR_CONFIG/AVR_EN	I	Analog/CMOS	ADDR_CONFIG_AVR_EN – Combined ADDR_CONFIG and AVR_EN pin, this pin works as ADDR_CONFIG during VDD ramping up, after address is latched, works as AVR_EN. ADDR_CONFIG – Combined ADDR and CONFIG pin, this pin works as ADDR during VDD ramping up when the top and bottom resistors are installed, as CONFIG when the bottom resistor is installed only. AVR_EN – This pin used as Active High Enable for the Rail A.

23	SVI3_RESET#	I	CMOS	Active low signal causing all SVI3 state machines and SVI3-defined registers to reset to default states.
24	SVI3_VDDIO	I	Power	VDDIO powers and serves as the reference the SVI3 interface pins: SVD, SVTI and SVTO, needs a decoupling cap of $\geq 1\mu\text{F}$ to GND.
25	BVR_RDY	O	Open Drain	Active high, Power Good output asserts when the output voltage of Rail B is in regulation.
26	SVI3_SVD	I	CMOS	Serial VID Data is a push-pull signal which transmits commands from the master to the slaves.
27	SVI3_SVC	I	CMOS	Serial VID Clock is a push-pull signal which acts as a clock for SVD, SVTI and SVTO.
28	SVI3_SVTO	O	CMOS	Serial VID Telemetry Output is a push-pull output driven by each slave. It carries telemetry and acknowledge packets.
29	SVI3_SVTI	I	CMOS	Serial VID Telemetry Input is driven by the next-furthest slave (from the master) on the telemetry daisy-chain. It carries telemetry and acknowledge packets.
30	CVR_RDY	O	Open Drain	Active high, Power Good output asserts when the output voltage of Rail C is in regulation.
31	AVSP	I	Analog	Rail A output remote voltage sense at the load point
32	AVSN	I	Analog	Rail A GND remote voltage sense at the load point
33	ISEN1	I	Analog	Current Sense of Phase 1
34	ISEN2			Current Sense of Phase 2
35	ISEN3			Current Sense of Phase 3
36	ISEN4			Current Sense of Phase 4
37	ISEN5			Current Sense of Phase 5
38	ISEN6			Current Sense of Phase 6
39	ISEN7			Current Sense of Phase 7
40	ISEN8			Current Sense of Phase 8
41	ISEN9			Current Sense of Phase 9
42	ISEN10			Current Sense of Phase 10
43	ISEN11			Current Sense of Phase 11
44	ISEN12			Current Sense of Phase 12
45	ISEN13			Current Sense of Phase 13
46	ISEN14			Current Sense of Phase 14
47	ISEN15			Current Sense of Phase 15
48	ISEN16			Current Sense of Phase 16
49	BVSN	I	Analog	Rail B GND remote voltage sense at the load point
50	BVSP	I	Analog	Rail B output remote voltage sense at the load point
51	CVSN	I	Analog	Rail C GND remote voltage sense at the load point
52	CVSP	I	Analog	Rail C output remote voltage sense at the load point
53	BVR_EN/VR_FLT#/S_MB_ALT#	I/O	Open Drain/C MOS	BVR_EN – This pin used as Active High Enable for the Rail B. VR_FLT# – Active low catastrophic fault pin indicator, controller stops regulating when this pin is pulled low.

				SMB_ALT# – PMBus active low ALERT# signal.
54	TSENC/VR_FLT#/SM B_ALT#	I/ O	Open Drain/C MOS	TSENC – Temperature Sense input from all the phases of Rail C VR_FLT# – Active low catastrophic fault pin indicator, controller stops regulating when this pin is pulled low. SMB_ALT# – PMBus active low ALERT# signal.
55	TSENB/VR_FLT#/SM B_ALT#	I/ O	Open Drain/C MOS	TSENB – Temperature Sense input from all the phases of Rail B VR_FLT# – Active low catastrophic fault pin indicator, controller stops regulating when this pin is pulled low. SMB_ALT# – PMBus active low ALERT# signal.
56	TSENA/VR_FLT#/SM B_ALT#	I/ O	Open Drain/C MOS	TSENA – Temperature Sense input from all the phases of Rail A VR_FLT# – Active low catastrophic fault pin indicator, controller stops regulating when this pin is pulled low. SMB_ALT# – PMBus active low ALERT# signal.
57	ISYS/IINSEN/PSYS	I	Analog	ISYS/IINSEN – input current sense, pull a resistor to GND on this pin and not exceeding VREF (1.5V) PSYS – input power per system, pull a resistor to GND on this pin and not exceeding VREF (1.5V)
58	VSYS/VINSEN	I	Analog	To sense input voltage of power stages with a resistive voltage divider (1/6), needs a decoupling cap of 0.1uF to GND. This pin also represents the VSYS.
59	VDD	I	Power	3.3V supply voltage input. Needs a decoupling cap of $\geq 1\mu\text{F}$ to GND
60	VREF	O	Power	1.5V reference voltage output. Needs a decoupling cap of $1\mu\text{F}$ to GND, but not greater than $4.7\mu\text{F}$
*	Thermal Pad	I	Ground	Ground pad, tie to GND plane with vias.

When TOP_CHIP_CFG_52[3:0]=101b(AVS), the pinout becomes as follows:



ASIC (AVSBus)				
PIN		I/ O	Type	DESCRIPTION
No.	NAME			
1	PWM16/VR_FLT#/SMB_ALT#	O	3.3V CMOS / Open Drain	PWM16 – PWM signal for Phase 16 VR_FLT# – Active low catastrophic fault pin indicator, controller stops regulating when this pin is pulled low. SMB_ALT# – PMBus active low ALERT# signal.
2	PWM15		PWM signal for Phase 15	
3	PWM14		PWM signal for Phase 14	
4	PWM13		PWM signal for Phase 13	
5	PWM12		PWM signal for Phase 12	
6	PWM11		PWM signal for Phase 11	
7	PWM10		PWM signal for Phase 10	
8	PWM9		PWM signal for Phase 9	
9	PWM8		PWM signal for Phase 8	
10	PWM7		PWM signal for Phase 7	
11	PWM6		PWM signal for Phase 6	
12	PWM5		PWM signal for Phase 5	
13	PWM4		PWM signal for Phase 4	
14	PWM3		PWM signal for Phase 3	
15	PWM2		PWM signal for Phase 2	
16	PWM1		PWM signal for Phase 1	
17	VRAMP_C1	O	Open Drain	Active low whenever the railA's output voltage is settled. This pin will hold high if the Vboot target has not reached during boot or if a new VID is set but not yet reached.
18	SMB_SDA	I/ O	Open Drain	PMBus bi-directional serial data signal.
19	SMB_SCL	I	Open Drain	PMBus serial clock signal.
20	VR_FLT#/SMB_ALT#/CVR_EN	I/ O	Open Drain/C MOS	VR_FLT# – Active low catastrophic fault pin indicator, controller stops regulating when this pin is pulled low. SMB_ALT# – PMBus active low ALERT# signal. CVR_EN – This pin used as Active High Enable for the Rail C.
21	AVR_RDY	O	Open Drain	Active high, Power Good output asserts when the output voltage of Rail A is in regulation.
22	ADDR_CONFIG_AVR_EN/ADDR_CONFIG/AVR_EN	I	Analog/CMOS	ADDR_CONFIG_AVR_EN – Combined ADDR_CONFIG and AVR_EN pin, this pin works as ADDR_CONFIG during VDD ramping up, after address is latched, works as AVR_EN. ADDR_CONFIG – Combined ADDR and CONFIG pin, this pin works as ADDR during VDD ramping up when the top and bottom resistors are installed, as CONFIG when the bottom resistor is installed only. AVR_EN – This pin used as Active High Enable for the Rail A.

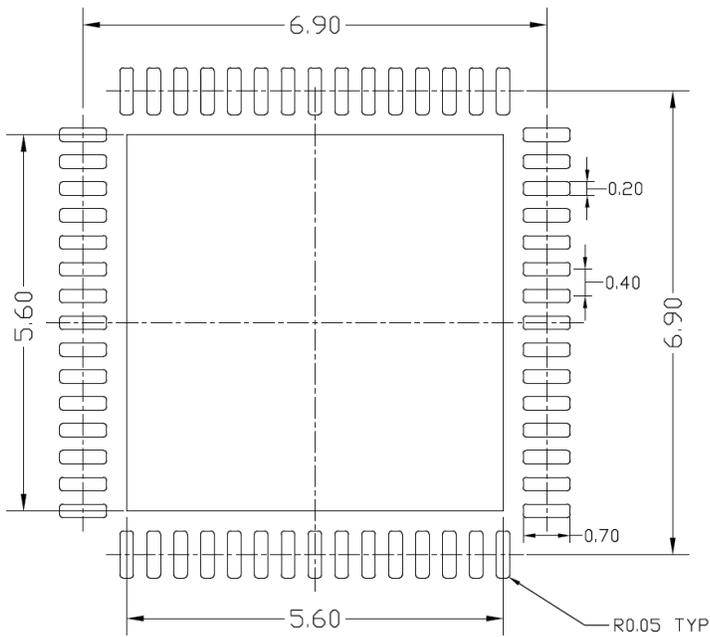
23	VRAMP_C2	O	Open Drain	Active low whenever the railB's output voltage is settled. This pin will hold high if the Vboot target has not reached during boot or if a new VID is set but not yet reached.
24	AVS_VDDIO	I	Power	VDDIO powers and serves as the reference the AVSBus interface pins: AVS_CLK, AVS_MDAT and AVS_SDAT.
25	BVR_RDY	O	Open Drain	Active high, Power Good output asserts when the output voltage of Rail B is in regulation.
26	AVS_MDAT	I	CMOS	AVSBus master data input.
27	AVS_CLK	I	CMOS	AVSBus clock input.
28	AVS_SDAT	I/O	CMOS	AVSBus slave data output.
29	VRAMP_C3	O	Open Drain	Active low whenever the railC's output voltage is settled. This pin will hold high if the Vboot target has not reached during boot or if a new VID is set but not yet reached.
30	CVR_RDY	O	Open Drain	Active high, Power Good output asserts when the output voltage of Rail C is in regulation.
31	AVSP	I	Analog	Rail A output remote voltage sense at the load point
32	AVSN	I	Analog	Rail A GND remote voltage sense at the load point
33	ISEN1	I	Analog	Current Sense of Phase 1
34	ISEN2			Current Sense of Phase 2
35	ISEN3			Current Sense of Phase 3
36	ISEN4			Current Sense of Phase 4
37	ISEN5			Current Sense of Phase 5
38	ISEN6			Current Sense of Phase 6
39	ISEN7			Current Sense of Phase 7
40	ISEN8			Current Sense of Phase 8
41	ISEN9			Current Sense of Phase 9
42	ISEN10			Current Sense of Phase 10
43	ISEN11			Current Sense of Phase 11
44	ISEN12			Current Sense of Phase 12
45	ISEN13			Current Sense of Phase 13
46	ISEN14			Current Sense of Phase 14
47	ISEN15			Current Sense of Phase 15
48	ISEN16			Current Sense of Phase 16
49	BVSN	I	Analog	Rail B GND remote voltage sense at the load point
50	BVSP	I	Analog	Rail B output remote voltage sense at the load point
51	CVSN	I	Analog	Rail C GND remote voltage sense at the load point
52	CVSP	I	Analog	Rail C output remote voltage sense at the load point
53	BVR_EN/VR_FLT#/SMB_ALT#	I/O	Open Drain/CMOS	BVR_EN – This pin used as Active High Enable for the Rail B. VR_FLT# – Active low catastrophic fault pin indicator, controller stops regulating when this pin is pulled low. SMB_ALT# – PMBus active low ALERT# signal.

54	TSENC/VR_FLT#/SM B_ALT#	I/ O	Open Drain/C MOS	TSENC – Temperature Sense input from all the phases of Rail C VR_FLT# – Active low catastrophic fault pin indicator, controller stops regulating when this pin is pulled low. SMB_ALT# – PMBus active low ALERT# signal.
55	TSENB/VR_FLT#/SM B_ALT#	I/ O	Open Drain/C MOS	TSENB – Temperature Sense input from all the phases of Rail B VR_FLT# – Active low catastrophic fault pin indicator, controller stops regulating when this pin is pulled low. SMB_ALT# – PMBus active low ALERT# signal.
56	TSENA/VR_FLT#/SM B_ALT#	I/ O	Open Drain/C MOS	TSENA – Temperature Sense input from all the phases of Rail A VR_FLT# – Active low catastrophic fault pin indicator, controller stops regulating when this pin is pulled low. SMB_ALT# – PMBus active low ALERT# signal.
57	ISYS/IINSEN/PSYS	I	Analog	ISYS/IINSEN – input current sense, pull a resistor to GND on this pin and not exceeding VREF (1.5V) PSYS – input power per system, pull a resistor to GND on this pin and not exceeding VREF (1.5V)
58	VSYS/VINSEN	I	Analog	To sense input voltage of power stages with a resistive voltage divider (1/6), needs a decoupling cap of 0.1uF to GND. This pin also represents the VSYS.
59	VDD	I	Power	3.3V supply voltage input. Needs a decoupling cap of $\geq 1\mu\text{F}$ to GND
60	VREF	O	Power	1.5V reference voltage output. Needs a decoupling cap of $1\mu\text{F}$ to GND, but not greater than $4.7\mu\text{F}$
*	Thermal Pad	I	Ground	Ground pad, tie to GND plane with vias.

Ordering Information

Part Number	Package	Shipping Method	Package Marking
RS18G30R	QFN-60	3ku Tape & Reel	R18G30

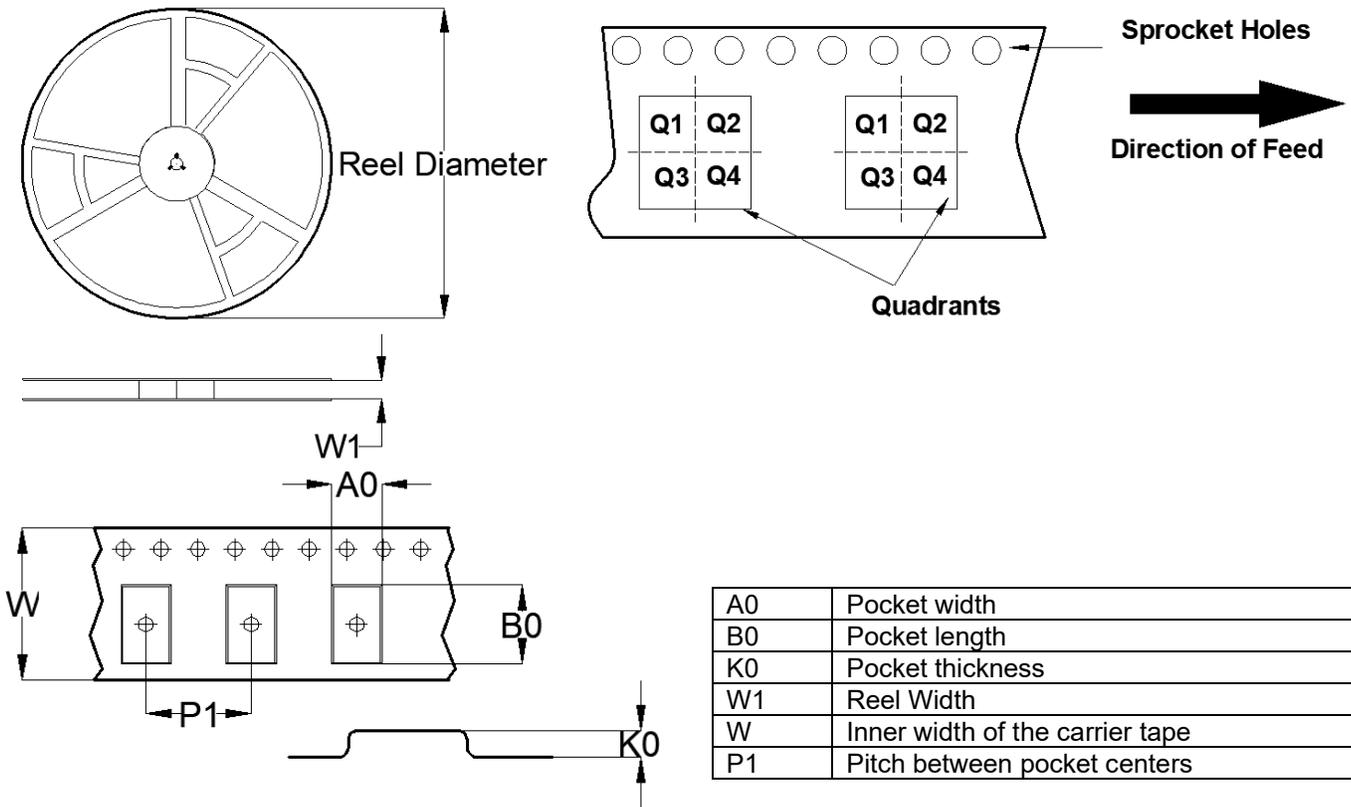
Recommended Land Pattern



NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 3) JEDEC REFERENCE IS M0-220.
- 4) DRAWING IS NOT TO SCALE.

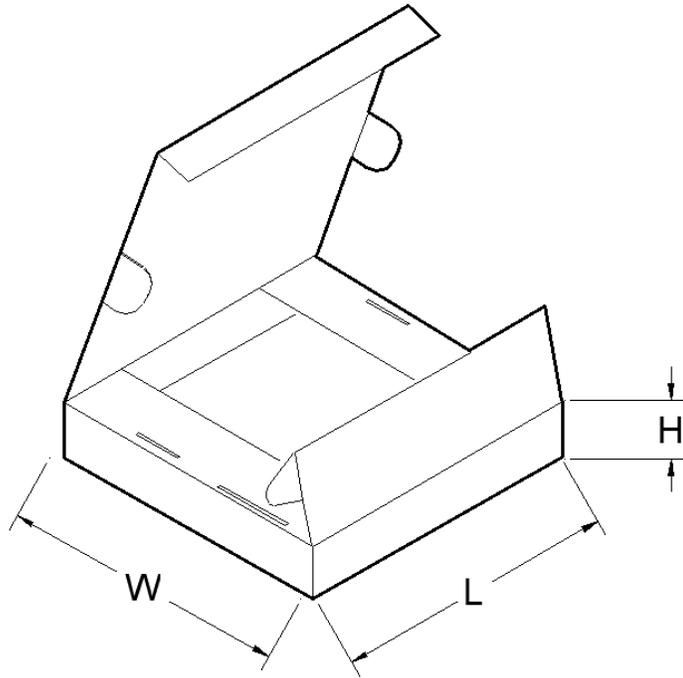
Tape and Reel Information



PKG type(mm)	Reel Diameter(mm)	Reel Width W1(mm)	A0(mm)	B0(mm)	K0(mm)	P1(mm)	W(mm)	Quad
7x7	330	16	7.3	7.3	1.1	12	16	Q2

*All the data is nominal

Pizza Box Dimension



PKG type(mm)	Units/box	Length(mm)	Width(mm)	Height(mm)
7x7	3000	354	337	55

*All the data is nominal