RS16630 Triple-Channel (N+M+O<= 6 Phase) Step-Down Multiphase Controller with AVSBus and PMBus™ Interface

Features

- Native Trans-Inductor Voltage Regulator (TLVR) Support
  - No external passive components required
- Built-in 1kΩ current sense resistor
- Paired with ReedSemi Smart Power Stages or Modules for high density solutions
- Scalability and Flexibility
  - Scalable phase count: (6+0+0) to (2+2+2)
  - Flexible phase order assignment
- Input and Output Range, Accuracy
  - 4.5V to 16V input & 0.2V to 2.7V output
  - 0.5% accurate output with differential sense
- Telemetry
  - 1.5% Input & Output voltage accuracy
  - 1.5% Output current accuracy
  - +/-2°C Temperature accuracy
- Improved Performance
  - Improved efficiency: Programmable Auto phase add/drop thresholds for optimization
  - Programmable Over-shoot & Under-shoot Reduction thresholds for better transient
  - Thermal Balance Management
- Protection Capability
  - Programmable Fault Response: Latch & Hiccup
  - UVLO, UVP, OVP, OCP, OTP
  - Cycle by cycle per-phase current limit
- Output BOM, Platform Area and Cost Reduction
  - Up to 4MHz switching frequency & Constant On Time control with fast transient for smaller & low-cost external passives
  - Programmable DC load line helps reduce the overshoot and the external capacitors
- Ease-of-use, Interfaces and Debug Features
  - Internal compensation
  - PMBus™ v1.4.1 Compliant/AVSBus 1.4/2.0 Compliant
  - Built in Multiple time Programmability (MTP) with up to 31 writes for field programmability
  - Black box registers for fault record
- RoHS Compliant and Green
- 6 mm × 6 mm, 52-Pin, QFN Package

Applications

- Server and Telecom Voltage Regulators
- Graphic Card Core Regulators
- Power Module

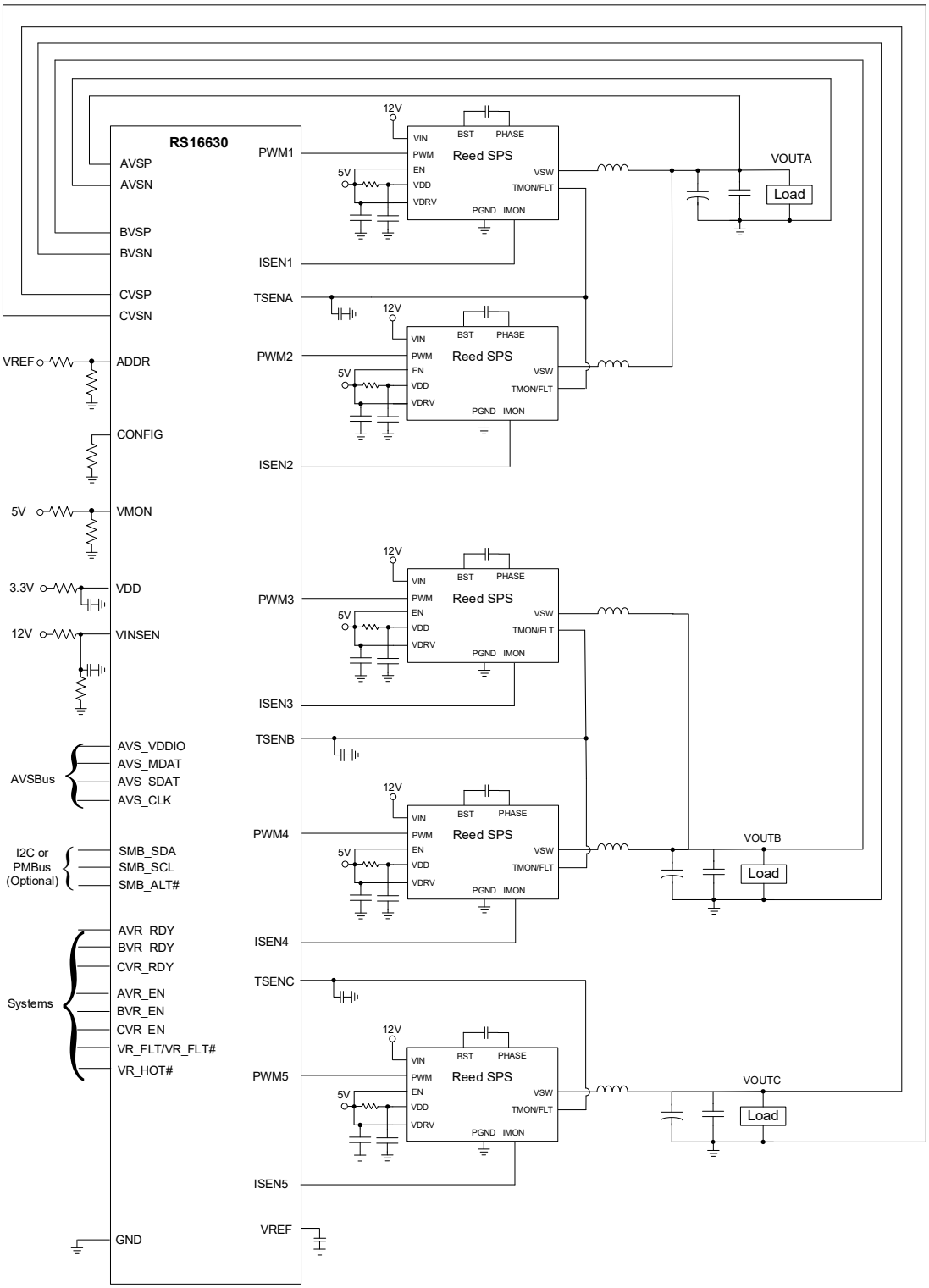
Description

RS16630 is a AVSBus compliant triple output multiphase buck controller with built-in MTP & PMBus™ interface. It is fully compatible with Reed Semiconductor's smart power stage. Advanced control features such as programmable DC load line, undershoot & overshoot reduction provide fast transient response hence needing low output capacitance. The device also provides auto phase add/drop with phase current balancing for efficiency improvement across loads. It supports fast dynamic voltage transitions with programable slew rates. All programmable parameters can be configured by the PMBus interface and can be stored in devices as default values. The MTP gives an added advantage of optimizing the device performance in the field.

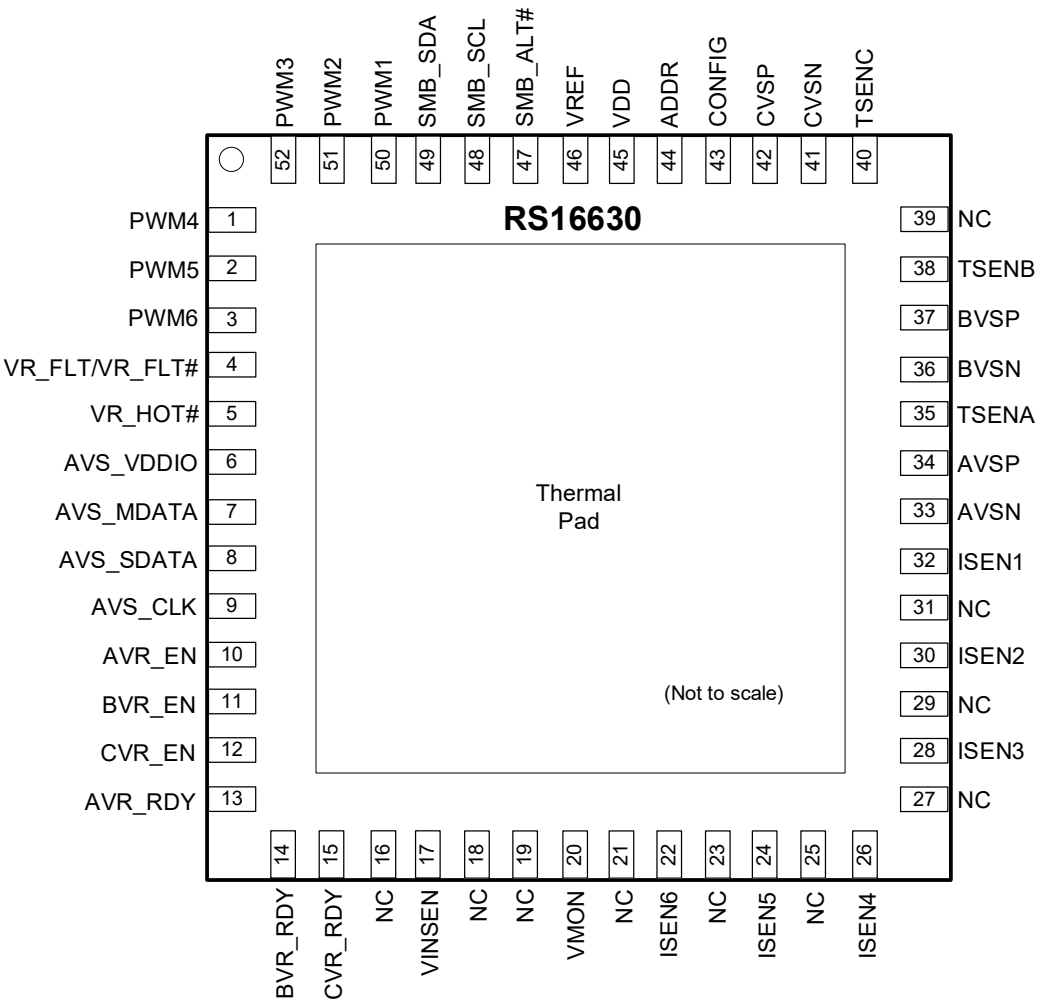
RS16630 is offered in a 52-pin QFN package and is rated to operate from -40°C to 125°C

Typical Application Circuit

Application Example (2+2+1)



Pin Description List



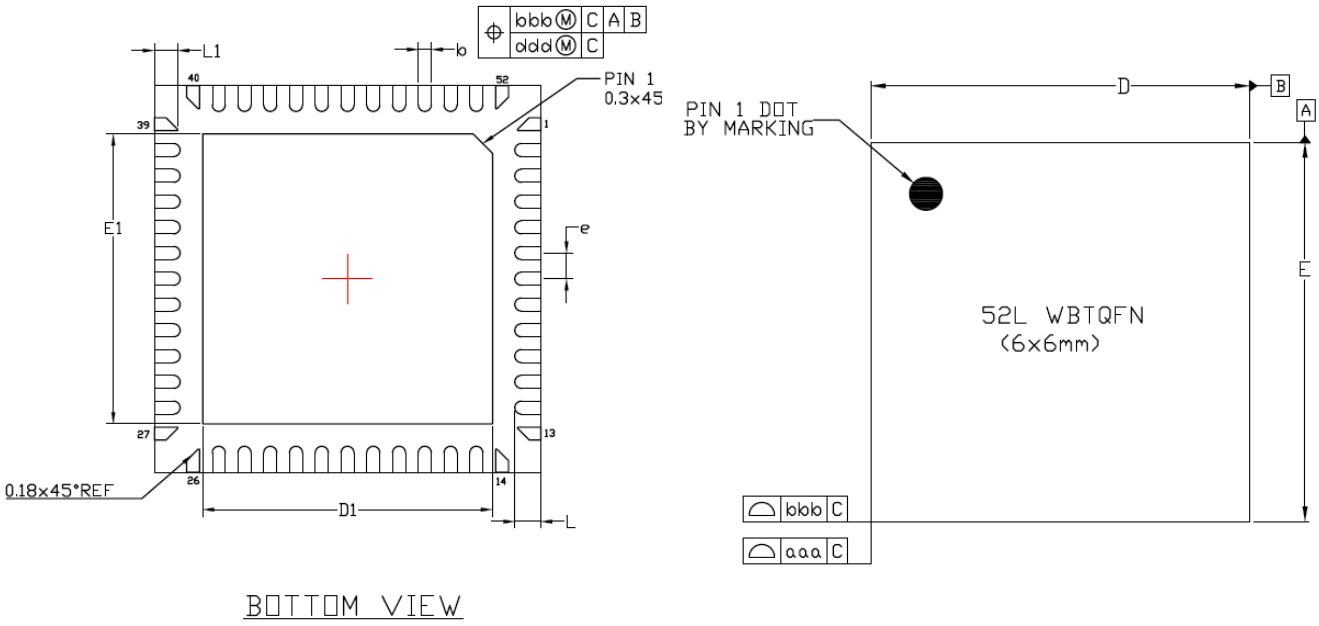
PIN		I/O	Type	DESCRIPTION
No.	NAME			
1	PWM4	O	3.3V CMOS	PWM signal for Phase 4
2	PWM5			PWM signal for Phase 5
3	PWM6			PWM signal for Phase 6
4	VR_FLT/VR_FLT#	O	CMOS/ Open Drain	This is a multi-function pin, can be configured as VR_FLT or VR_FLT# through MTP registers *VR_FLT – Active high catastrophic fault pin indicator, controller stops regulating when this pin is pulled high.* *VR_FLT# – Active low catastrophic fault pin indicator, controller stops regulating when this pin is pulled low.*
5	VR_HOT#	O	Open Drain	Active low smart power stage temperature indicator. VRHOT# is asserted at the temperature configured by (51h)OT_WARN_LIMIT.
6	AVS_VDDIO	I	CMOS	VDDIO (1.2V, 1.8V or 3.3V) powers and serves as the reference the AVSBus interface pins: AVS_CLK, AVS_MDAT and AVS_SDAT.
7	AVS_MDATA	I	CMOS	AVSBus master data input.
8	AVS_SDATA	I/O	CMOS	AVSBus slave data output.
9	AVS_CLK	I	CMOS	AVSBus clock input.
10	AVR_EN	I	CMOS	This pin used as Active High Enable for the Rail A.
11	BVR_EN	I	CMOS	This pin used as Active High Enable for the Rail B.
12	CVR_EN	I	CMOS	This pin used as Active High Enable for the Rail C.
13	AVR_RDY	O	Open Drain	Active high, Power Good output asserts when the output voltage of Rail A is in regulation.
14	BVR_RDY	O	Open Drain	Active high, Power Good output asserts when the output voltage of Rail B is in regulation.
15	CVR_RDY	O	Open Drain	Active high, Power Good output asserts when the output voltage of Rail C is in regulation.
16	NC			No connection internally
17	VINSEN	I	Analog	To sense input voltage of power stages with a resistive voltage divider (1/6), needs a decoupling cap of 0.1uF to GND
18	NC			No connection internally
19	NC			No connection internally
20	VMON	I	Analog	To sense driver voltage of power stages with a resistive voltage divider (1/5), needs a decoupling cap of 10nF to GND
21	NC			No connection internally
22	ISEN6	I	Analog	Current Sense of Phase 6
23	NC			No connection internally
24	ISEN5	I	Analog	Current Sense of Phase 5
25	NC			No connection internally
26	ISEN4	I	Analog	Current Sense of Phase 4

27	NC			No connection internally
28	ISEN3	I	Analog	Current Sense of Phase 3
29	NC			No connection internally
30	ISEN2	I	Analog	Current Sense of Phase 2
31	NC			No connection internally
32	ISEN1	I	Analog	Current Sense of Phase 1
33	AVSN	I	Analog	Rail A GND remote voltage sense at the load point
34	AVSP	I	Analog	Rail A output remote voltage sense at the load point
35	TSENA	I	Analog	Temperature Sense input from all the phases of Rail A
36	BVSN	I	Analog	Rail B GND remote voltage sense at the load point
37	BVSP	I	Analog	Rail B output remote voltage sense at the load point
38	TSENB	I	Analog	Temperature Sense input from all the phases of Rail B
39	NC			
40	TSENC	I	Analog	Temperature Sense input from all the phases of Rail C
41	CVSN	I	Analog	Rail C GND remote voltage sense at the load point
42	CVSP	I	Analog	Rail C output remote voltage sense at the load point
43	CONFIG	I	Analog	MTP configuration selection pins. Tie a resistor to GND to this pin
44	ADDR	I	Analog	An external resistor from ADDR to GND and another from VREF to ADDR sets the PMBus address. The address is latched at VDD power up.
45	VDD	I	Power	3.3V supply voltage input. Needs a decoupling cap of ≥1μF to GND
46	VREF	O	Power	1.5V reference voltage output. Needs a decoupling cap of 1μF to GND, but not greater than 4.7μF
47	SMB_ALT#	O	Open Drain	PMBus active low ALERT# signal.
48	SMB_SCL	I	Open Drain	PMBus serial clock signal.
49	SMB_SDA	I/O	Open Drain	PMBus bi-directional serial data signal.
50	PWM1	O	3.3V CMOS	PWM signal for Phase 1
51	PWM2			PWM signal for Phase 2
52	PWM3			PWM signal for Phase 3
*	Thermal Pad	I	Ground	Ground pad, tie to GND plane with vias.

Ordering Information

Part Number	Package	Shipping Method	Package Marking
RS16630R	QFN-52	3ku Tape & Reel	R16630

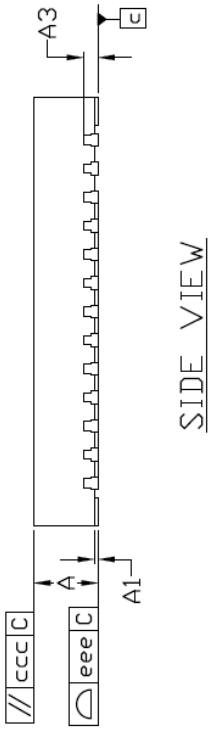
Package information



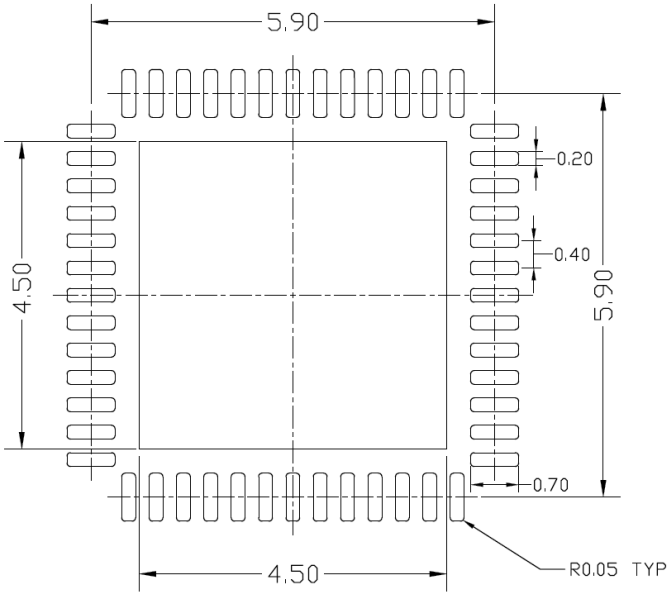
Notes

1. All DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER JEDEC MO-220.
3. DRAWING IS NOT TO SCALE.

Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	---	---	0.05
A3	0.203 Ref.		
D	5.90	6.00	6.10
E	5.90	6.00	6.10
D1	4.45	4.50	4.55
E1	4.45	4.50	4.55
b	0.15	0.20	0.25
e	0.40BSC		
L	0.35	0.40	0.45
L1	0.31	0.36	0.41
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		



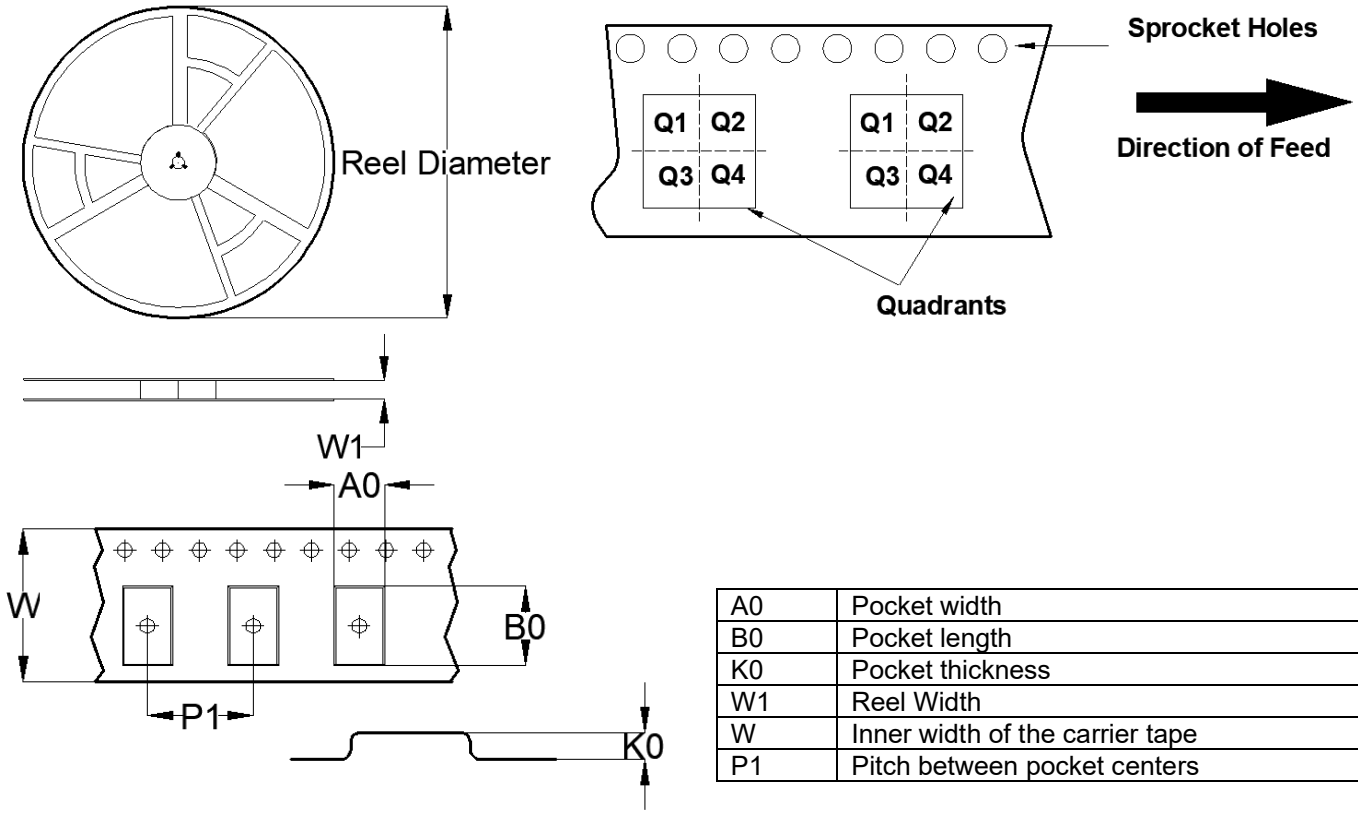
Recommended Land Pattern



NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

Tape and Reel Information

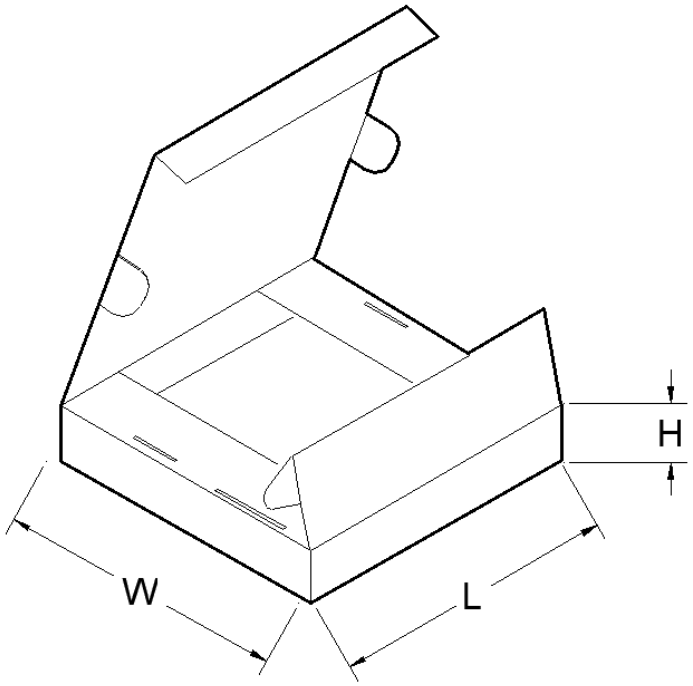


A0	Pocket width
B0	Pocket length
K0	Pocket thickness
W1	Reel Width
W	Inner width of the carrier tape
P1	Pitch between pocket centers

PKG type(mm)	Reel Diameter(mm)	Reel Width W1(mm)	A0(mm)	B0(mm)	K0(mm)	P1(mm)	W(mm)	Quad
6x6	330	16	6.3	6.3	1.1	12	16	Q2

*All the data is nominal

Pizza Box Dimension



PKG type(mm)	Units/box	Length(mm)	Width(mm)	Height(mm)
6x6	3000	354	337	55

*All the data is nominal