RS16K20 Dual-Channel (N+M<= 20 Phase) Step-Down Multiphase Controller with AVSBus and PMBus™ Interface

Features

- Native Trans-Inductor Voltage Regulator (TLVR) Support
  - No external passive components required
- Built-in 1kΩ current sense resistor
- Paired with ReedSemi Smart Power Stages or Modules for high density solutions
- Scalability and Flexibility
  - Scalable phase count: (20+0) to (10+10)
  - Flexible phase order assignment
- Input and Output Range, Accuracy
  - 4.5V to 16V input & 0.2V to 2.7V output
  - 0.5% accurate output with differential sense
- Telemetry
  - 1.5% Input & Output voltage accuracy
  - 1.5% Output current accuracy
  - +/-2°C Temperature accuracy
- Improved Performance
  - Improved efficiency: Programmable Auto phase add/drop thresholds for optimization
  - Programmable Over-shoot & Under-shoot Reduction thresholds for better transient
  - Thermal Balance Management
- Protection Capability
  - Programmable Fault Response: Latch & Hiccup
  - UVLO, UVP, OVP, OCP, OTP
  - Cycle by cycle per-phase current limit
- Output BOM, Platform Area and Cost Reduction
  - Up to 4MHz switching frequency & Constant On Time control with fast transient for smaller & low-cost external passives
  - Programmable DC load line helps reduce the overshoot and the external capacitors
- Ease-of-use, Interfaces and Debug Features
  - Internal compensation
  - AVSBus™ revision 1.4/2.0 Compliant
  - PMBus™ v1.4.1 Compliant
  - Built in Multiple time Programmability (MTP) with up to 31 writes for field programmability
  - Black box registers for fault record
- RoHS Compliant and Green
- 8 mm × 8 mm, 68-Pin, QFN Package

Applications

- Server and Telecom Voltage Regulators
- Graphic Card Core Regulators
- Power Module

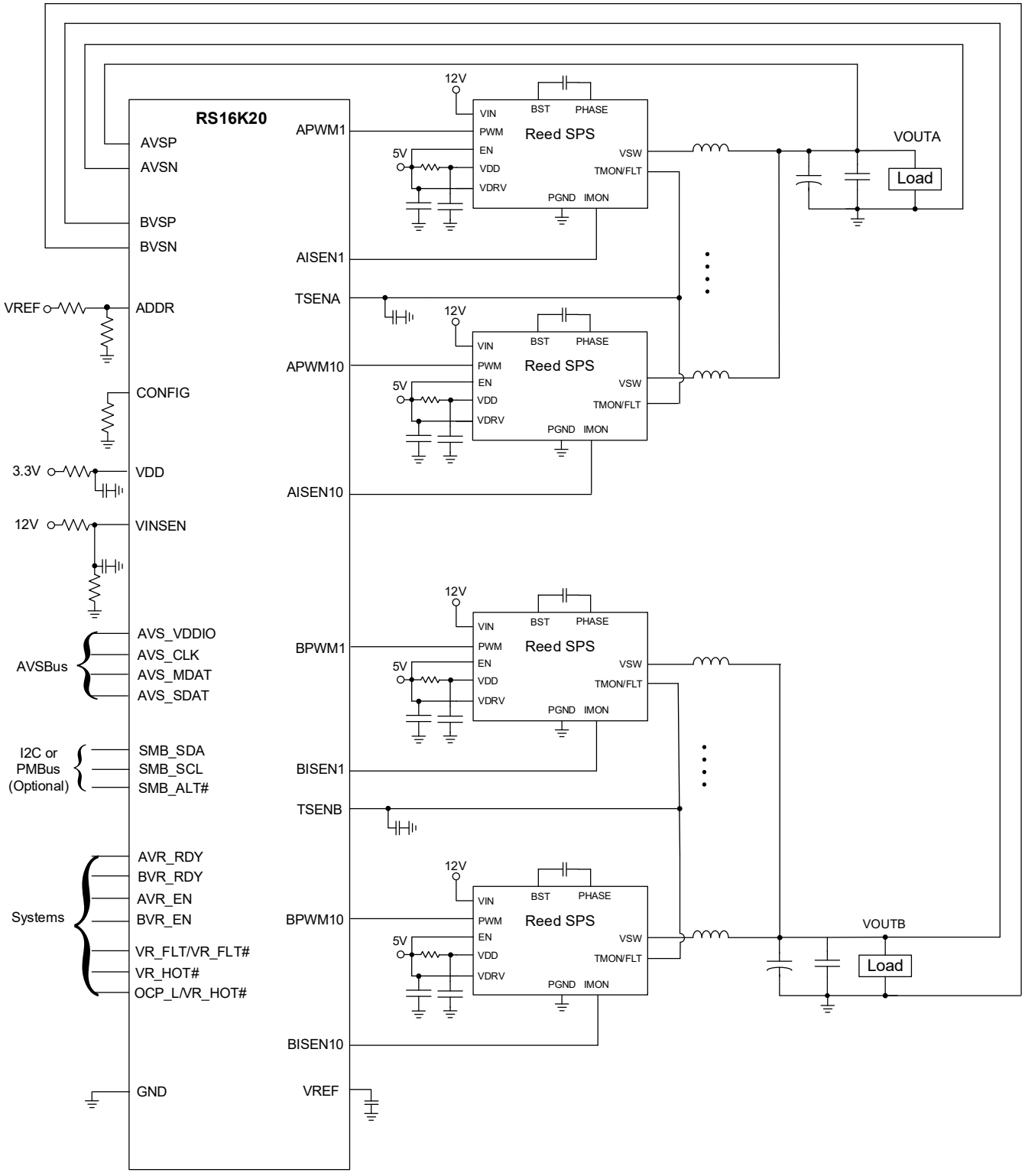
Descriptions

RS16K20 is a AVSBus™ compliant dual output multiphase buck controller with built-in MTP & PMBus™ interface. It is fully compatible with Reed Semiconductor's smart power stage. Advanced control features such as programmable DC load line, undershoot & overshoot reduction provide fast transient response hence needing low output capacitance. The device also provides auto phase add/drop with phase current balancing for efficiency improvement across loads. It supports fast dynamic voltage transitions with programable slew rates. All programmable parameters can be configured by the PMBus interface and can be stored in devices as default values. The MTP gives an added advantage of optimizing the device performance in the field.

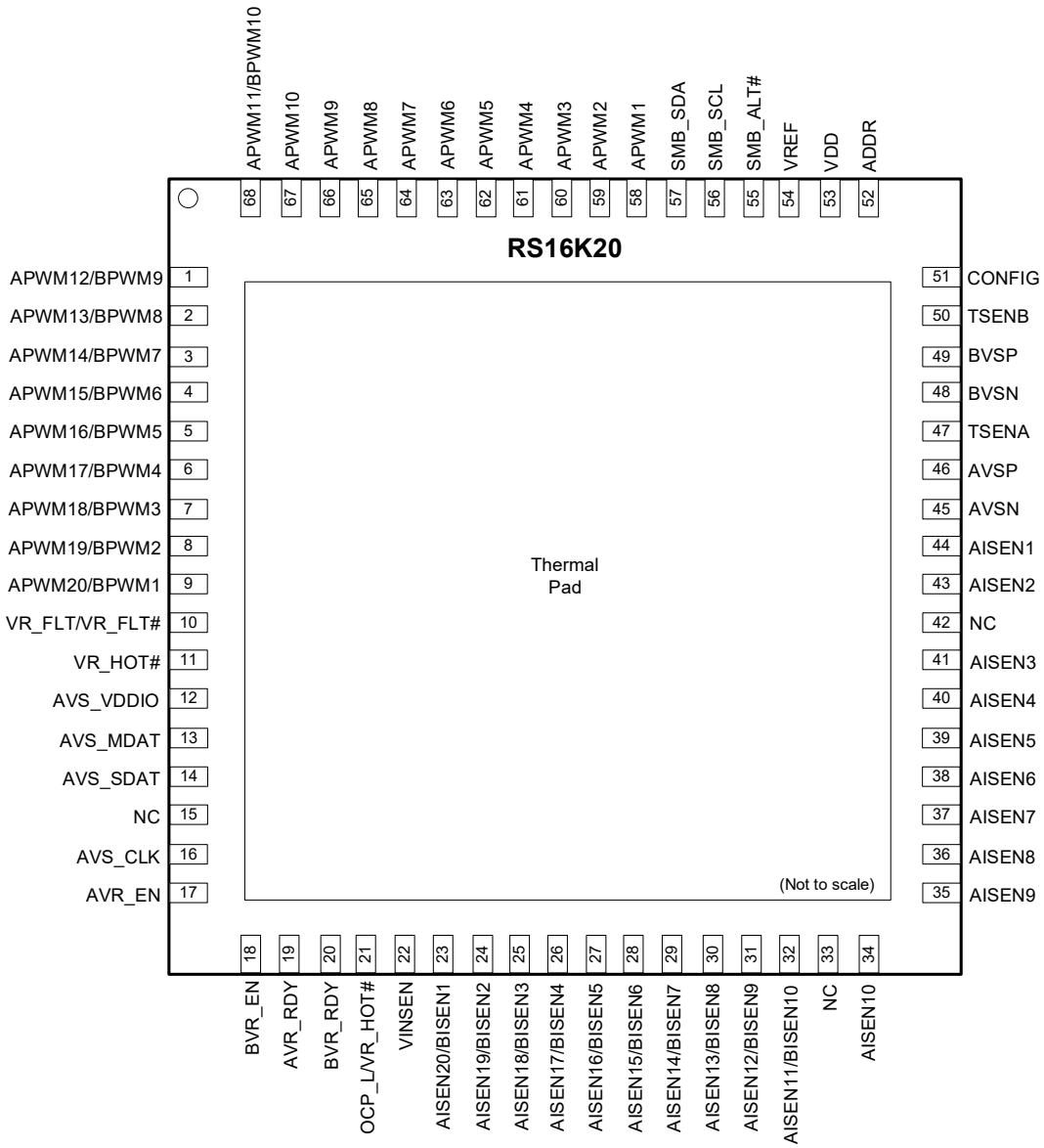
RS16K20 is offered in a 68-pin QFN package and is rated to operate from -40°C to 125°C

Typical Application Diagram

Application Example (10+10)



Pin Description List



PIN		I/O	Type	DESCRIPTION	
No.	NAME				
1	APWM12/BPWM9	O	3.3V CMOS	PWM signal for Phase 12 of Rail A/Phase 9 of RailB	**Tri-state logic level:** 0V: Low Side FET ON 3.3V: High Side FET ON Tri-state (tied to VREF): Both FETs OFF If unused, leave them floating
2	APWM13/BPWM8			PWM signal for Phase 13 of Rail A/Phase 8 of RailB	
3	APWM14/BPWM7			PWM signal for Phase 14 of Rail A/Phase 7 of RailB	
4	APWM15/BPWM6			PWM signal for Phase 15 of Rail A/Phase 6 of RailB	
5	APWM16/BPWM5			PWM signal for Phase 16 of Rail A/Phase 5 of RailB	
6	APWM17/BPWM4			PWM signal for Phase 17 of Rail A/Phase 4 of RailB	
7	APWM18/BPWM3			PWM signal for Phase 18 of Rail A/Phase 3 of RailB	
8	APWM19/BPWM2			PWM signal for Phase 19 of Rail A/Phase 2 of RailB	
9	APWM20/BPWM1			PWM signal for Phase 20 of Rail A/Phase 1 of RailB	
10	VR_FLT/VR_FLT#	O	CMOS/ Open Drain	Active high catastrophic fault pin indicator, controller stops regulating when this pin is pulled high. To have an option to select active low, open-drain output or active high, CMOS output	
11	VR_HOT#	O	Open Drain	Active low smart power stage temperature indicator. VRHOT# is asserted at the temperature configured by (51h)OT_WARN_LIMIT.	
12	AVS_VDDIO	I	CMOS	VDDIO (1.2V or , 1.8V or 3.3V) powers and serves as the reference the AVSBus interface pins: AVS_CLK, AVS_MDAT and AVS_SDAT.	
13	AVS_MDAT	I	CMOS	AVSBus master data input.	
14	AVS_SDAT	I/O	CMOS	AVSBus slave data output.	
15	NC			No connection internally	
16	AVS_CLK	I	CMOS	AVSBus clock input.	
17	AVR_EN	I	CMOS	This pin used as Active High Enable for the Rail A.	
18	BVR_EN	I	CMOS	This pin used as Active High Enable for the Rail B.	
19	AVR_RDY	O	Open Drain	Active high, Power Good output asserts when the output voltage of Rail A is in regulation.	
20	BVR_RDY	O	Open Drain	Active high, Power Good output asserts when the output voltage of Rail B is in regulation.	
21	OCP_L/ VR_HOT#	O	Open Drain	This is a multi-function pin, can be configured as OCP_L or VR_HOT# through MTP registers *OCP_L – Active low when output current exceeds the threshold* *VR_HOT# -- Active low smart power stage temperature indicator. VRHOT# is asserted at the temperature configured by (51h)OT_WARN_LIMIT.*	
22	VINSEN	I	Analog	To sense input voltage of power stages with a resistive voltage divider (1/6), needs a decoupling cap of 0.1uF to GND	
23	AISEN20/BISEN1	I	Analog	Current Sense of Rail A Phase 20/ Rail B Phase 1	If unused, leave them floating
24	AISEN19/BISEN2			Current Sense of Rail A Phase 19/ Rail B Phase 2	
25	AISEN18/BISEN3			Current Sense of Rail A Phase 18/ Rail B Phase 3	
26	AISEN17/BISEN4			Current Sense of Rail A Phase 17/ Rail B Phase 4	

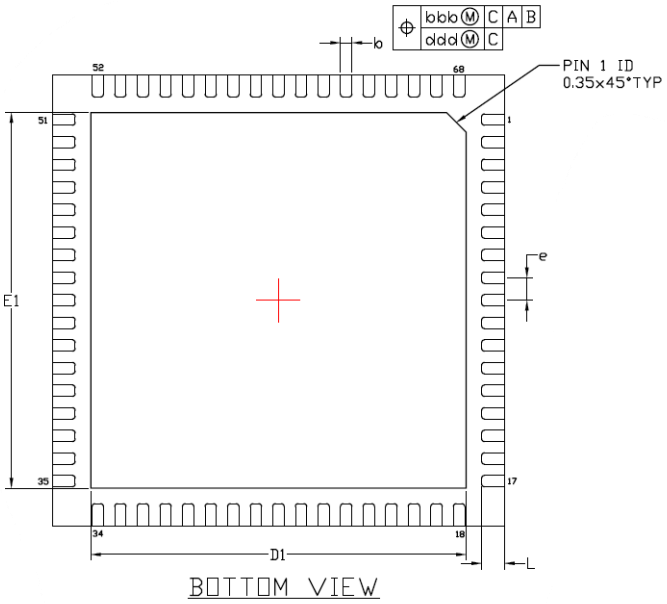
27	AISEN16/BISEN5			Current Sense of Rail A Phase 16/ Rail B Phase 5
28	AISEN15/BISEN6			Current Sense of Rail A Phase 15/ Rail B Phase 6
29	AISEN14/BISEN7			Current Sense of Rail A Phase 14/ Rail B Phase 7
30	AISEN13/BISEN8			Current Sense of Rail A Phase 13/ Rail B Phase 8
31	AISEN12/BISEN9			Current Sense of Rail A Phase 12/ Rail B Phase 9
32	AISEN11/BISEN10			Current Sense of Rail A Phase 11/ Rail B Phase 10
33	NC			No connection internally
34	AISEN10	I	Analog	Current Sense of Rail A Phase 10
35	AISEN9			Current Sense of Rail A Phase 9
36	AISEN8			Current Sense of Rail A Phase 8
37	AISEN7			Current Sense of Rail A Phase 7
38	AISEN6			Current Sense of Rail A Phase 6
39	AISEN5			Current Sense of Rail A Phase 5
40	AISEN4			Current Sense of Rail A Phase 4
41	AISEN3			Current Sense of Rail A Phase 3
42	NC			No connection internally
43	AISEN2	I	Analog	Current Sense of Rail A Phase 2
44	AISEN1			Current Sense of Rail A Phase 1
45	AVSN	I	Analog	Rail A GND remote voltage sense at the load point
46	AVSP	I	Analog	Rail A output remote voltage sense at the load point
47	TSENA	I	Analog	Temperature Sense input from all the phases of Rail A
48	BVSN	I	Analog	Rail B GND remote voltage sense at the load point
49	BVSP	I	Analog	Rail B output remote voltage sense at the load point
50	TSENB	I	Analog	Temperature Sense input from all the phases of Rail B
51	CONFIG	I	Analog	MTP configuration selection pins. Tie a resistor to GND to this pin
52	ADDR	I	Analog	An external resistor from ADDR to GND and another from VREF to ADDR sets the PMBus address. The address is latched at VDD power up.
53	VDD	I	Power	3.3V supply voltage input. Needs a decoupling cap of ≥1μF to GND
54	VREF	O	Power	1.5V reference voltage output. Needs a decoupling cap of 1μF to GND, but not greater than 4.7μF
55	SMB_ALT#	O	Open Drain	PMBus active low ALERT# signal.
56	SMB_SCL	I	Open Drain	PMBus serial clock signal.
57	SMB_SDA	I/O	Open Drain	PMBus bi-directional serial data signal.
58	APWM1	O	3.3V CMOS	PWM signal for Phase 1 of Rail A
59	APWM2			PWM signal for Phase 2 of Rail A
60	APWM3			PWM signal for Phase 3 of Rail A

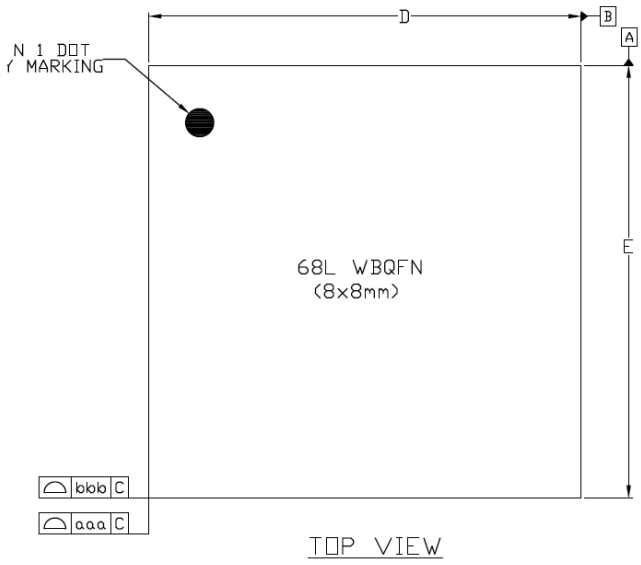
61	APWM4			PWM signal for Phase 4 of Rail A
62	APWM5			PWM signal for Phase 5 of Rail A
63	APWM6			PWM signal for Phase 6 of Rail A
64	APWM7			PWM signal for Phase 7 of Rail A
65	APWM8			PWM signal for Phase 8 of Rail A
66	APWM9			PWM signal for Phase 9 of Rail A
67	APWM10			PWM signal for Phase 10 of Rail A
68	APWM11/BPWM10			PWM signal for Phase 11 of Rail A/Phase 10 of RailB
*	Thermal Pad	I	Ground	Ground pad, tie to GND plane with vias.

Ordering Information

Part Number	Package	Shipping Method	Package Marking
RS16K20R	QFN-68	TBD Tape & Reel	R16K20

Package information



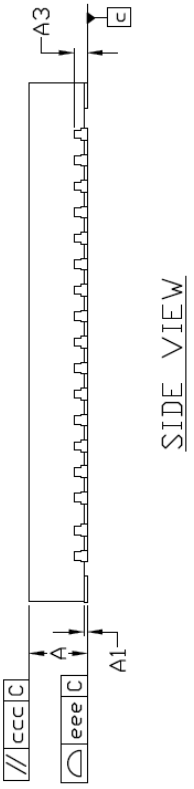


Notes

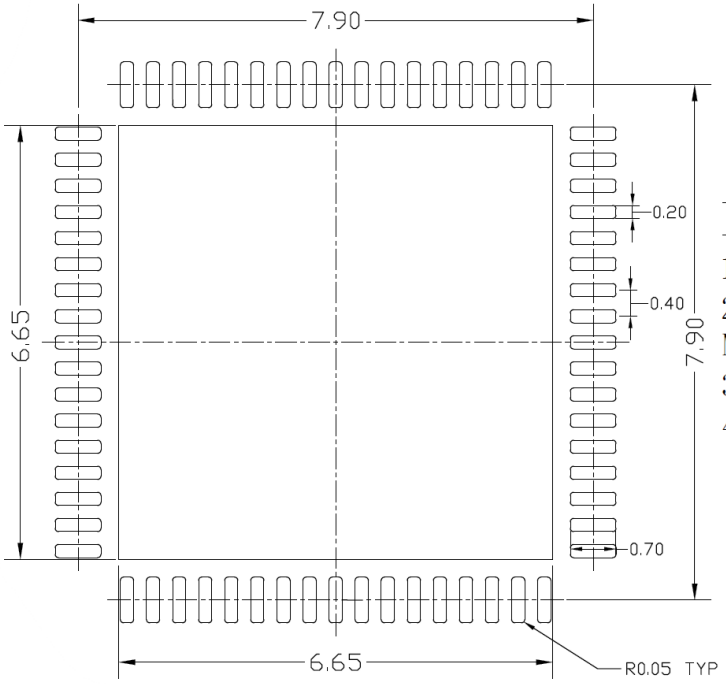
1. All DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER JEDEC MO-220.
3. DRAWING IS NOT TO SCALE.

Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.80	0.85	0.90
A1	---	---	0.05
A3	0.203 Ref.		
D	7.90	8.00	8.10
E	7.90	8.00	8.10
D1	6.60	6.65	6.70
E1	6.60	6.65	6.70
b	0.20	0.20	0.25
e	0.40BSC		
L	0.35	0.40	0.45

Tol. of Form&Position	
aaa	0.10
bbb	0.10
ccc	0.10
ddd	0.05
eee	0.08



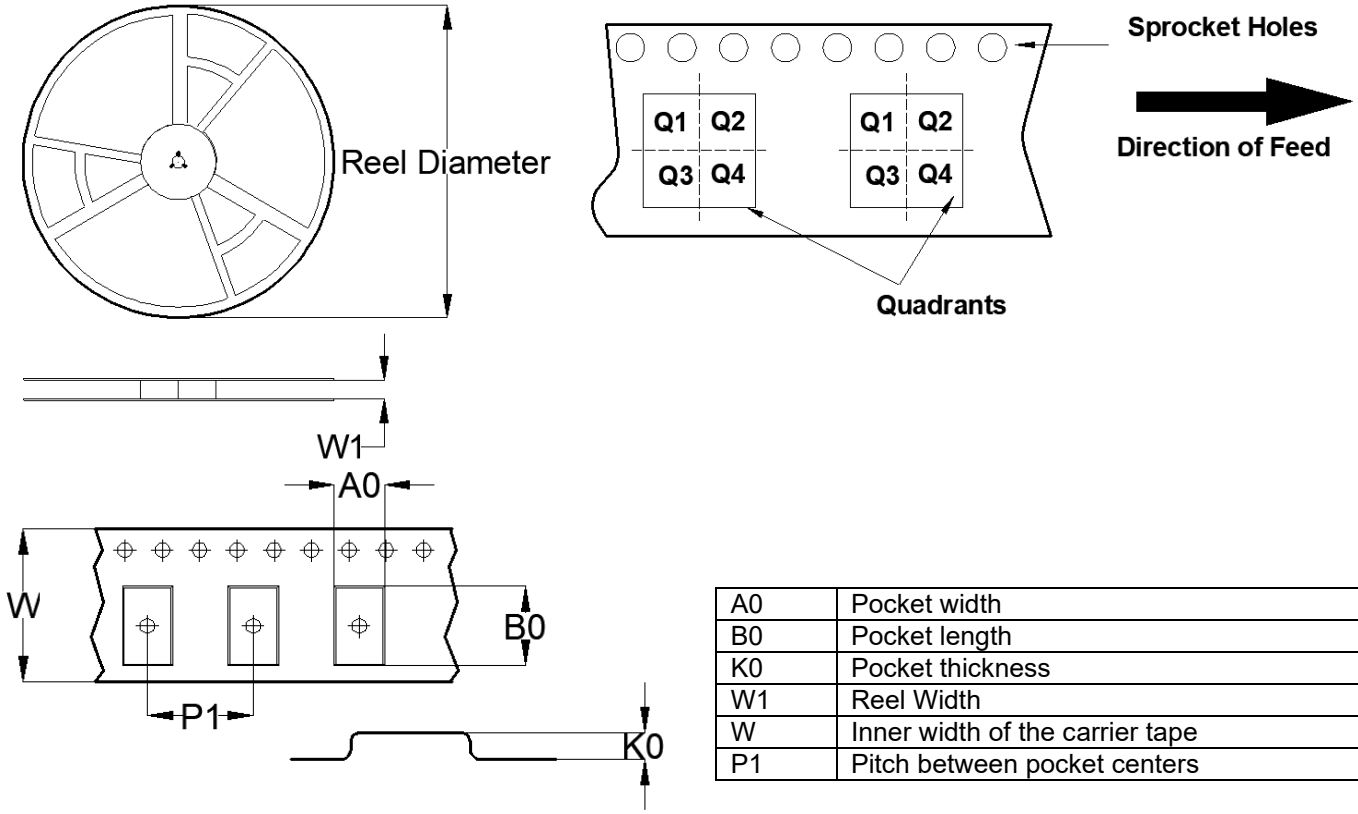
Recommended Land Pattern



NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

Tape and Reel Information

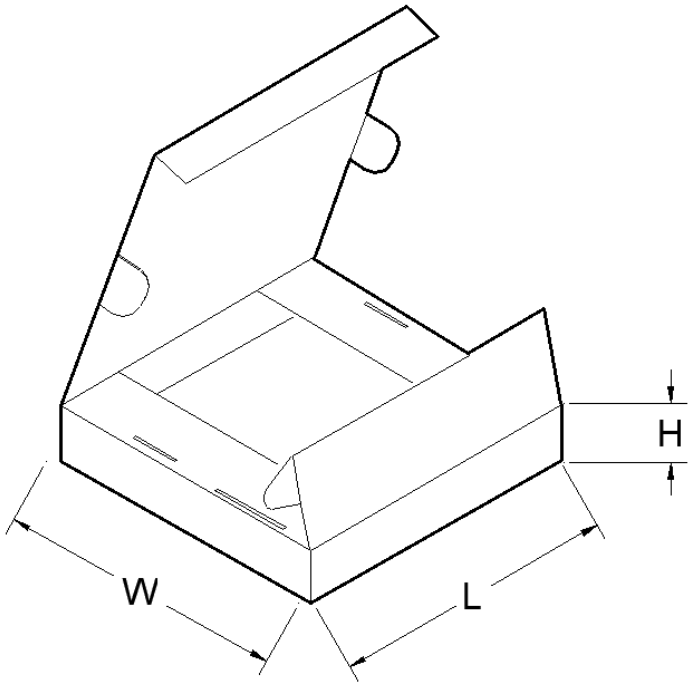


A0	Pocket width
B0	Pocket length
K0	Pocket thickness
W1	Reel Width
W	Inner width of the carrier tape
P1	Pitch between pocket centers

PKG type	Reel Diameter (mm)	Reel Width W1(mm)	A0(mm)	B0(mm)	K0(mm)	P1(mm)	W(mm)	Quad
8x8	330	16	8.3	8.3	1.1	12	16	Q2

*All the data is nominal

Pizza Box Dimension



PKG type	Units/box	Length(mm)	Width(mm)	Height(mm)
8x8	3000	354	337	55

*All the data is nominal