

RS19C22 – 12-Phase Dual-Rail TLVR Controller with SVI3 and PMBus

Features

Flexible 12-Phase Dual-Rail Architecture

- Up to 12 phases with flexible $N + M \leq 12$ allocation
 - Configurations from 12 + 0 to 8 + 4
- Flexible phase-order assignment
- Compatible with Reed Smart Power Stages and Smart Power Blocks

Native TLVR & Fast Transient Performance

- Native Trans-Inductor Voltage Regulator (TLVR) support
 - No additional external passive components required
 - Integrated 1k Ω current-sense resistor
- Programmable overshoot and undershoot reduction
- Automatic phase add/drop with programmable thresholds
- Thermal phase balancing
- Up to 4MHz switching frequency
- Constant-on-time control
- Programmable DC load line

Wide operating range and high-accuracy regulation

- 4.5V to 16V input; 0.2V to 2.8V output
- $\pm 0.5\%$ output-voltage accuracy with differential sensing
- Programmable load-line control

Integrated telemetry

- $\pm 1.5\%$ voltage and current accuracy
- $\pm 2^\circ\text{C}$ temperature accuracy

Comprehensive protection

- UVLO, UVP, OVP, OCP, and OTP
- Cycle-by-cycle per-phase current limiting
- Programmable latch-off or auto-retry fault response

Digital Interfaces, Configuration & Diagnostics

- AMD SVI3 compliant
- PMBus v1.4.1 compliant
- MTP with up to 32 writes for field programmability
- Black-box registers for fault recording

Package

- 6mm $\times$ 6mm, 48-pin QFN
- RoHS compliant and green

Applications

- Server and AI Computing Core Power
- CPU and GPU Core Power
- Graphics Cards
- High-Performance Computing
- Telecom Power Systems

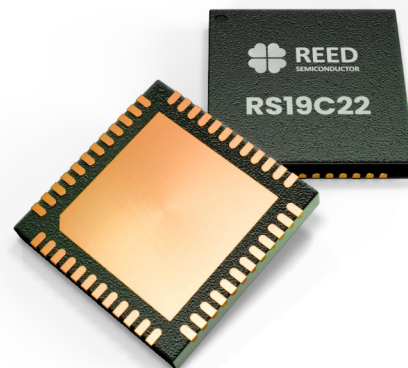
Description

The RS19C22 is a high-performance, dual-output digital multiphase controller supporting up to 12 phases with flexible $N + M \leq 12$ phase allocation. Designed for high-current computing, graphics, server, and telecom power applications, the device operates from 4.5V to 16V and supports output voltages from 0.2V to 2.8V with $\pm 0.5\%$ output-voltage accuracy.

Native TLVR support, constant-on-time control, programmable load-line regulation, and automatic phase add/drop provide fast transient response and efficient operation across changing load conditions. Switching frequencies up to 4MHz enable high-density power conversion, while programmable overshoot and undershoot reduction and thermal phase balancing further optimize transient and thermal performance.

Integrated voltage, current, and temperature telemetry provides real-time system monitoring. The RS19C22 supports AMD SVI3 and PMBus v1.4.1, with MTP configuration and black-box fault recording for system configuration and diagnostics. Integrated protection includes UVLO, UVP, OVP, OCP, OTP, cycle-by-cycle per-phase current limiting, and programmable latch-off or auto-retry fault response.

When paired with Reed [Smart Power Stages](#) or [Smart Power Blocks](#), the RS19C22 provides a scalable, high-density multiphase power solution for demanding processor and graphics core power rails. The device is offered in a 6mm $\times$ 6mm, 48-pin QFN package and operates from -40°C to 125°C .



The schematic diagram illustrates the RS19C22 power management IC, which is a multi-channel DC-DC converter. The IC is shown in a top-down view, with its internal components and pin connections detailed.

IC Internal Structure:

- Top Section:** Contains two **Reed SPS 1Φ** (Single Phase) converters. Each has inputs for **VDD**, **VIN**, **VDRV**, **BST**, **VSW**, **TMON/FLT**, **IMON**, **EN**, and **GND**. The **VIN** pins are connected to a 12V input, and the **VDRV** pins are connected to a 5V input. The **EN** pins are connected to a 5V input. The **TMON/FLT** pins are connected to a 5V input. The **IMON** pins are connected to a 5V input.
- Middle Section:** Labeled **Rail B Phases 1~2 (2 × SPS or 1 × SPB)**. It contains two **Reed SPB 2Φ** (Two Phase) converters. Each has inputs for **VIN**, **VDRV**, **IMON1**, **IMON2**, **TMON/FLT1**, **TMON/FLT2**, **VOUT1**, **VOUT2**, **EN1**, **EN2**, **PWM1**, **PWM2**, and **GND**. The **VIN** pins are connected to a 12V input, and the **VDRV** pins are connected to a 5V input. The **EN1** and **EN2** pins are connected to a 5V input. The **PWM1** and **PWM2** pins are connected to a 5V input. The **TMON/FLT1** and **TMON/FLT2** pins are connected to a 5V input. The **IMON1** and **IMON2** pins are connected to a 5V input.
- Bottom Section:** Contains two **Reed SPS 1Φ** converters, similar to the top section, with inputs for **VDD**, **VIN**, **VDRV**, **BST**, **VSW**, **TMON/FLT**, **IMON**, **EN**, and **GND**.

Pin Connections:

- Top Pins:** **AVSP**, **AVSN**, **ADDR**, **VDD**, **I_{IN}_N**, **I_{IN}_P**, **SVI3_RESET#**, **SVI3_VDDIO**, **SVI3_SVD**, **SVI3_SVC**, **SVI3_SVTO**, **SVI3_SVTI**, **OCF#**, **SMB_SDA**, **SMB_SCL**, **AVR_EN**, **BVR_EN**.
- Left Pins:** **12V**, **VREF**, **3.3V**, **GND**.
- Right Pins:** **LoadA**, **LoadB**, **AVR_RDY**, **BVR_RDY**, **VR_FLT#**, **VR_HOT#**.
- Bottom Pins:** **BVSP**, **BVSN**, **GND**.

External Components:

- Capacitors:** Various electrolytic and ceramic capacitors are connected to the **VIN**, **VDRV**, **VSW**, **TMON/FLT**, **IMON**, **VOUT1**, **VOUT2**, **EN1**, **EN2**, **PWM1**, **PWM2**, **TMON/FLT1**, **TMON/FLT2**, **IMON1**, **IMON2**, **EN**, and **GND** pins.
- Resistors:** Various resistors are connected to the **VREF**, **3.3V**, **ADDR**, **OCF#**, **SMB_SDA**, **SMB_SCL**, **AVR_EN**, **BVR_EN**, **AVR_RDY**, **BVR_RDY**, **VR_FLT#**, and **VR_HOT#** pins.
- Switches:** Two switches, labeled **ON** and **OFF**, are connected to the **AVR_EN** and **BVR_EN** pins.

Ordering Information

PART NUMBER	PACKAGE	SIZE	MSL RATING	SHIPPING METHOD	PACKAGE MARKING
RS19C22R	QFN-48	6 × 6mm		3000u Tape & Reel	R19C22

Top Marking

Line 1

- RS: Prefix of Reed Semiconductor (R is replaced by E for engineering lots)
- YY: Year code
- WW: Week code

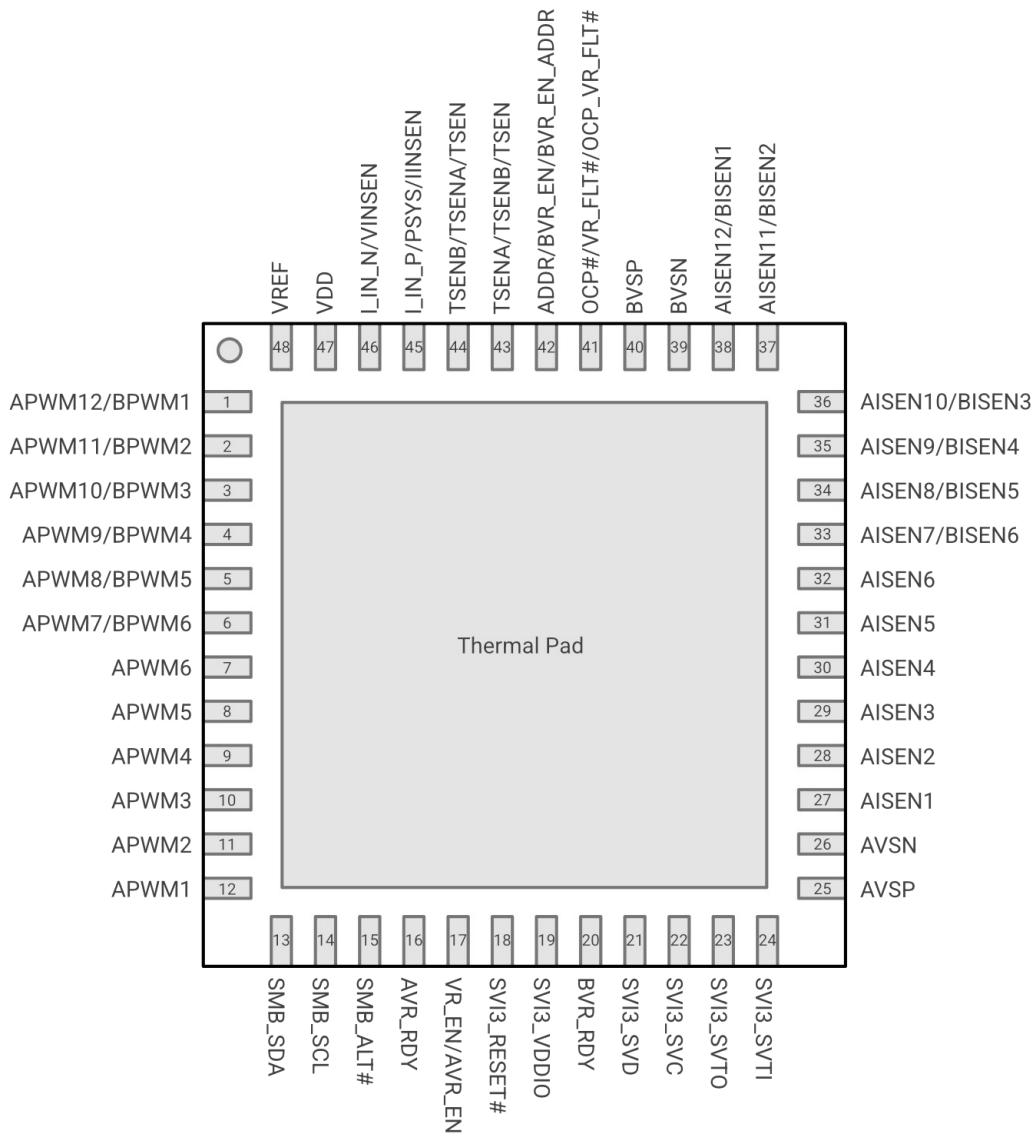
Line 2

- PPPPP: Truncated part number

Line 3

- LLLLL: Lot code
- S: Assembly site code

Package Reference



QFN-48(6 × 6mm)

Pin Descriptions

PIN	NAME	TYPE	DESCRIPTION
1	APWM12/ BPWM1	O	PWM output for Rail A Phase 12 or Rail B Phase 1.
2	APWM11/ BPWM2	O	PWM output for Rail A Phase 11 or Rail B Phase 2.
3	APWM10/ BPWM3	O	PWM output for Rail A Phase 10 or Rail B Phase 3.
4	APWM9/ BPWM4	O	PWM output for Rail A Phase 9 or Rail B Phase 4.
5	APWM8/ BPWM5	O	PWM output for Rail A Phase 8 or Rail B Phase 5.
6	APWM7/ BPWM6	O	PWM output for Rail A Phase 7 or Rail B Phase 6.
7	APWM6	O	PWM output for Rail A Phase 6.
8	APWM5	O	PWM output for Rail A Phase 5.
9	APWM4	O	PWM output for Rail A Phase 4.
10	APWM3	O	PWM output for Rail A Phase 3
11	APWM2	O	PWM output for Rail A Phase 2.
12	APWM1	O	PWM output for Rail A Phase 1.
13	SMB_SDA	I/O	PMBus bidirectional serial data.
14	SMB_SCL	I	PMBus serial clock input.
15	BVR_EN/ SMB_ALT#	O	Multifunction pin configurable through MTP as BVR_EN or SMB_ALT#. BVR_EN: Active-high Rail B enable input. SMB_ALT#: Active-low, open-drain PMBus ALERT# output.
16	AVR_RDY	O	Active-high, open-drain Power Good output. Asserts when Rail A output voltage is in regulation.
17	VR_EN/ AVR_EN	I	Multifunction enable input configurable through MTP as VR_EN or AVR_EN. VR_EN: Active-high enable input for Rails A and B. AVR_EN: Active-high Rail A enable input.
18	SVI3_RESET#	I	Active-low SVI3 reset input. Resets the SVI3 state machines and SVI3-defined registers to their default states.
19	SVI3_VDDIO	P	SVI3 interface supply and I/O reference voltage. Connect a $\geq 1\mu\text{F}$ decoupling capacitor from SVI3_VDDIO to GND.
20	BVR_RDY	O	Active-high, open-drain Power Good output. Asserts when Rail B output voltage is in regulation.
21	SVI3_SVD	I	SVI3 Serial VID Data input. Push-pull signal carrying command data from the host to the device.
22	SVI3_SVC	I	SVI3 Serial VID Clock input. Push-pull clock for SVI3_SVD, SVI3_SVTI, and SVI3_SVTO.
23	SVI3_SVTO	O	SVI3 Serial VID Telemetry Output. Push-pull output carrying telemetry and acknowledge packets.
24	SVI3_SVTI	I	SVI3 Serial VID Telemetry Input. Push-pull input receiving telemetry and acknowledge packets from the next device in the SVI3 telemetry daisy chain.
25	AVSP	I	Rail A positive remote-sense input. Connect to the output voltage at the point of regulation.
26	AVSN	I	Rail A negative remote-sense input. Connect to the output voltage at the point of regulation.

PWM outputs (Pins 1–12): 3.3V CMOS tri-state outputs. Low: low-side FET ON; High: high-side FET ON; Tri-state: both FETs OFF. If unused, leave floating.

Type: I = Input, O = Output, I/O = Bidirectional, P = Power, G = Ground, – = No Connect.

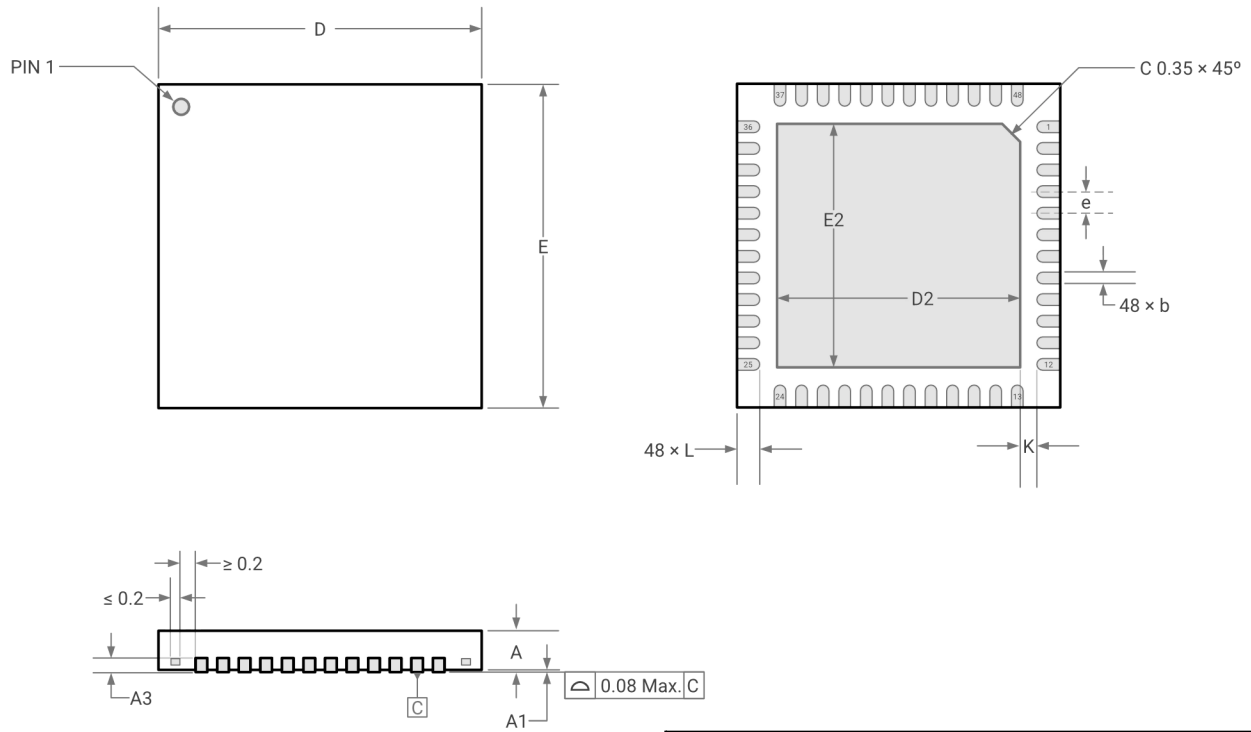
Pin Descriptions

PIN	NAME	TYPE	DESCRIPTION
27	AISEN1	I	Current-sense input for Rail A Phase 1.
28	AISEN2	I	Current-sense input for Rail A Phase 2.
29	AISEN3	I	Current-sense input for Rail A Phase 3.
30	AISEN4	I	Current-sense input for Rail A Phase 4.
31	AISEN5	I	Current-sense input for Rail A Phase 5.
32	AISEN6	I	Current-sense input for Rail A Phase 6.
33	AISEN7/ BISEN6	I	Current-sense input for Rail A Phase 7 or Rail B Phase 6.
34	AISEN8/ BISEN5	I	Current-sense input for Rail A Phase 8 or Rail B Phase 5.
35	AISEN9/ BISEN4	I	Current-sense input for Rail A Phase 9 or Rail B Phase 4.
36	AISEN10/ BISEN3	I	Current-sense input for Rail A Phase 10 or Rail B Phase 3.
37	AISEN11/ BISEN2	I	Current-sense input for Rail A Phase 11 or Rail B Phase 2.
38	AISEN12/ BISEN1	I	Current-sense input for Rail A Phase 12 or Rail B Phase 1.
39	BVSN	I	Rail B negative remote-sense input. Connect to the load ground at the point of regulation.
40	BVSP	I	Rail B positive remote-sense input. Connect to the output voltage at the point of regulation.
41	OCP#/ VR_FLT#/ OCP_VR_ FLT#	O	Configurable active-low, open-drain OCP and/or VR fault output. See Applications section for configuration details.
42	ADDR/BVR_ EN/BVR_EN_ ADDR	I	Configurable PMBus address-select and/or Rail B enable input. See Applications section for configuration details.
43	TSENA/ TSENB/TSEN	I	Configurable temperature-sense input for Rail A, Rail B, or both rails. See Applications section for configuration details.
44	TSENB/ TSENA/TSEN	I	Configurable temperature-sense input for Rail B, Rail A, or both rails. See Applications section for configuration details.
45	I_IN_P/PSYS/ IINSEN	I	Configurable input-current or system-power sense input. See Applications section for configuration details.
46	I_IN_N/ VINSEN	I	Configurable negative input-current sense or power-stage input-voltage sense input.
47	VDD	P	3.3V supply input. Connect a 1µF or larger ceramic bypass capacitor to GND.
48	VREF	O	1.5V reference-voltage output. Connect a 1µF decoupling capacitor to GND.
—	Thermal Pad	G	Exposed thermal pad. Connect to the GND plane with multiple thermal vias.

Type: I = Input, O = Output, I/O = Bidirectional, P = Power, G = Ground, — = No Connect.

Multifunction pins are configured through MTP registers. See the Applications section for configuration and connection details.

Package Dimensions



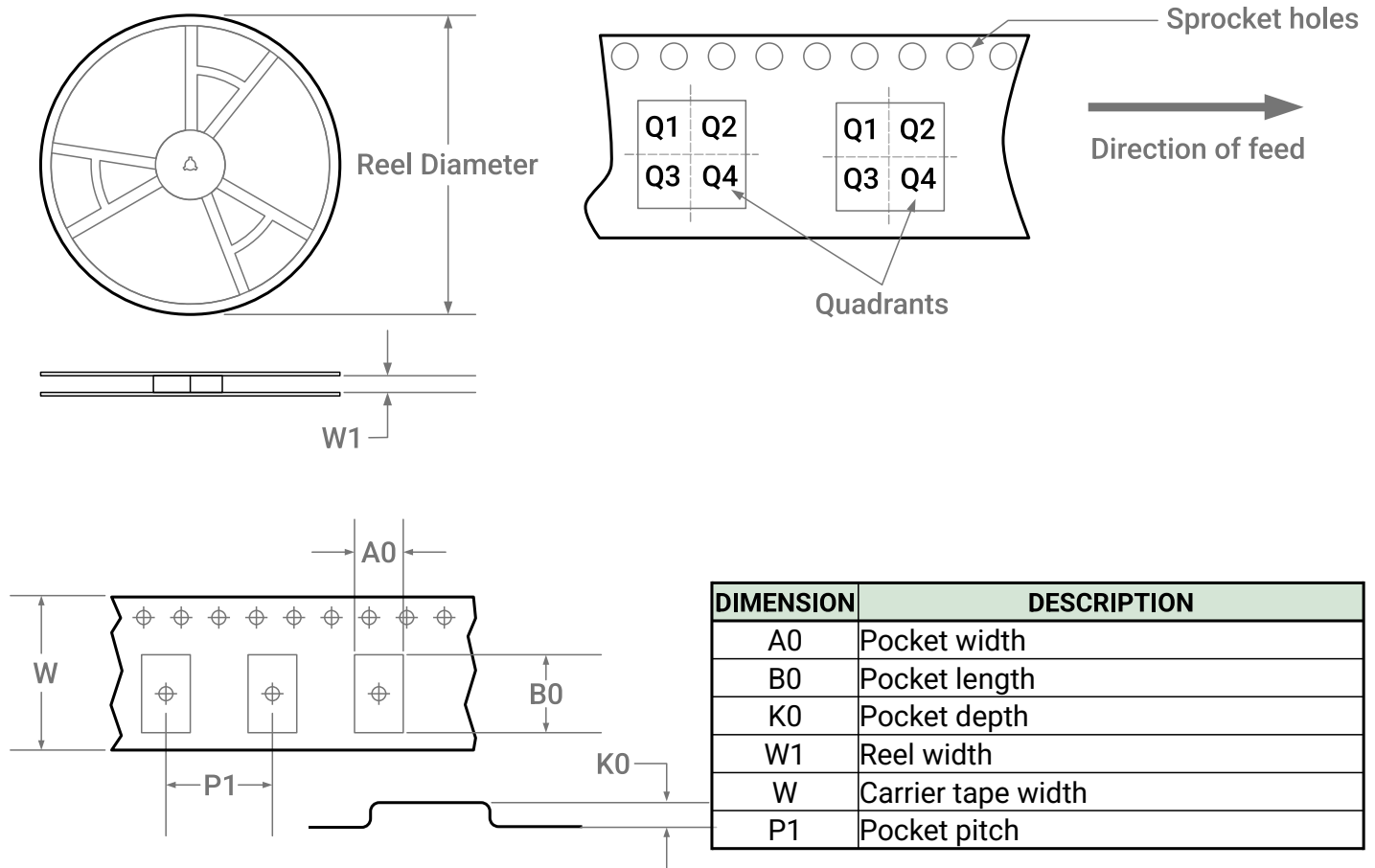
Notes

1. All dimensions are in millimeters.
2. Drawing per JEDEC MO-220.
3. Dimension b applies to the metallized terminal and is measured 0.15mm to 0.30mm from the terminal tip. If an optional terminal radius is present, dimension b does not apply within the radius area.
4. The bilateral coplanarity zone applies to both the exposed thermal pad and the terminals.
5. Drawing is not to scale.

REF	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 Ref.		
D	6.00 BSC		
E	6.00 BSC		
D2	4.35	4.40	4.45
E2	4.35	4.40	4.45
b	0.15	0.20	0.25
e	0.40 BSC		
L	0.30	0.40	0.50
K	0.20	—	—

1. All dimensions are in millimeters.
2. Drawing is not to scale.

Tape and Reel Information

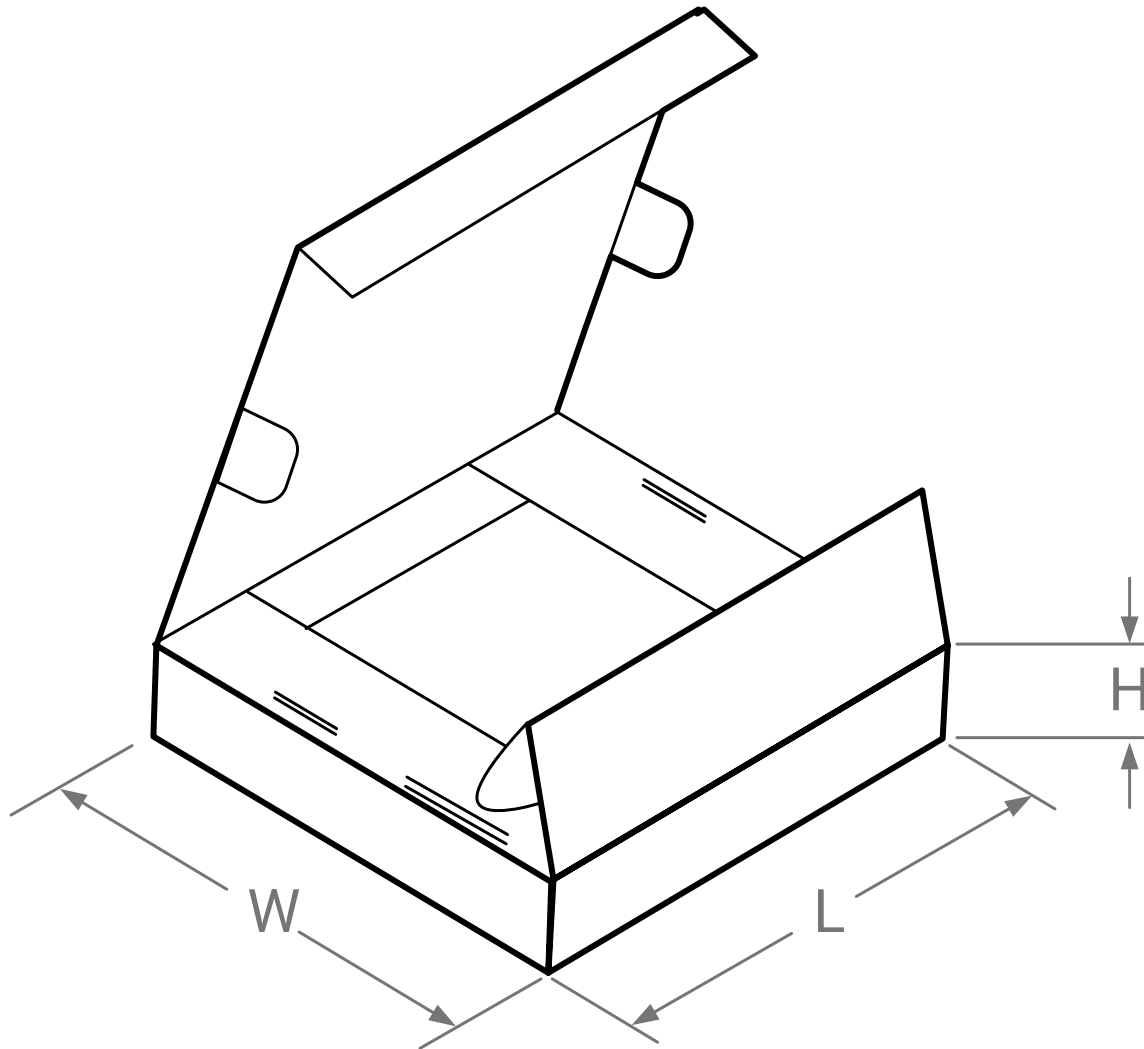


PACKAGE SIZE	REEL DIAMETER	W1	A0	B0	K0	P1	W	QUADRANT
6 × 6	330	16	6.3	6.3	1.10	12	16	Q2

Note:

1. All dimensions are nominal
2. All dimensions are in millimeters (mm)

Pizza Box Dimensions



PACKAGE SIZE	UNITS / BOX	LENGTH	WIDTH	HEIGHT
6 × 6	3000	367	367	38

Notes:

1. All measurements are in millimeters;
2. All measurements are nominal.