

RS19822 – 8-Phase Dual-Rail TLVR Controller with SVI3 and PMBus

Features

Flexible 8-Phase Dual-Rail Architecture

- Up to 8 phases with flexible $N + M \leq 8$ allocation
 - Configurations from 8 + 0 to 4 + 4
- Flexible phase-order assignment
- Compatible with Reed Smart Power Stages and Smart Power Blocks

Native TLVR & Fast Transient Performance

- Native Trans-Inductor Voltage Regulator (TLVR) support
 - No additional external passive components required
 - Integrated 1k Ω current-sense resistor
- Programmable overshoot and undershoot reduction
- Automatic phase add/drop with programmable thresholds
- Thermal phase balancing
- Up to 4MHz switching frequency
- Constant-on-time control
- Programmable DC load line

Wide operating range and high-accuracy regulation

- 4.5V to 16V input; 0.2V to 2.8V output
- $\pm 0.5\%$ output-voltage accuracy with differential sensing
- Programmable load-line control

Integrated telemetry

- $\pm 1.5\%$ voltage and current accuracy
- $\pm 2^\circ\text{C}$ temperature accuracy

Comprehensive protection

- UVLO, UVP, OVP, OCP, and OTP
- Cycle-by-cycle per-phase current limiting
- Programmable latch-off or auto-retry fault response

SVI3, PMBus, Configuration & Diagnostics

- AMD SVI3 compliant
- PMBus v1.4.1 compliant
- MTP with up to 32 configuration writes
- Black-box fault recording
- Internal compensation

Package

- 5mm $\times$ 5mm, 40-pin QFN package
- RoHS compliant and green

Applications

- AI Accelerator, GPU, and CPU Core Power
- FPGA and ASIC Core Power
- Server, HPC, and Networking Systems
- High-Current Power Modules

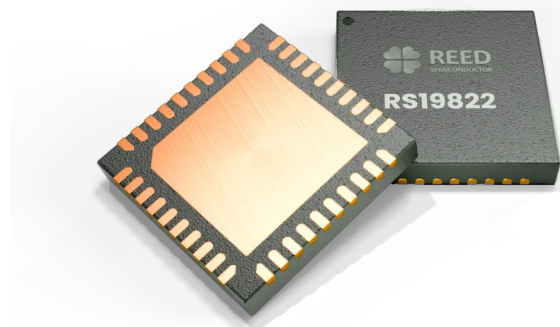
Description

The RS19822 is a high-performance, dual-rail digital multiphase controller supporting up to 8 phases with flexible $N + M \leq 8$ phase allocation. Designed for high-current computing and graphics core power applications, the device operates from 4.5V to 16V and supports output voltages from 0.2V to 2.8V with $\pm 0.5\%$ output-voltage accuracy.

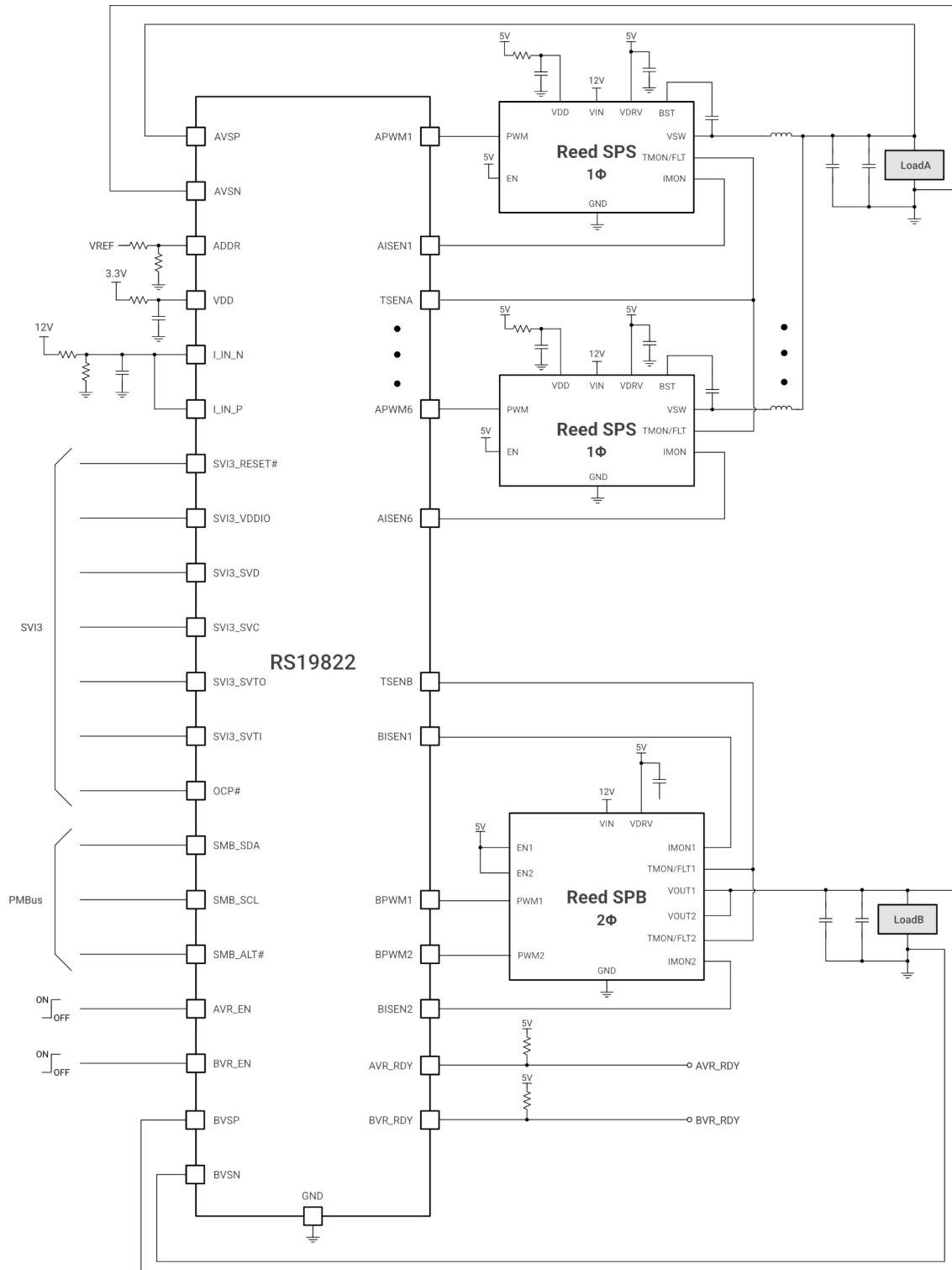
Native TLVR support, constant-on-time control, programmable load-line regulation, and automatic phase add/drop provide fast transient response and efficient operation across changing load conditions. Switching frequencies up to 4MHz enable high-density power conversion, while programmable overshoot and undershoot reduction and thermal phase balancing further optimize transient and thermal performance.

Integrated voltage, current, and temperature telemetry provides real-time system monitoring. The RS19822 supports AMD SVI3 and PMBus v1.4.1, with MTP configuration and black-box fault recording for system configuration and diagnostics. Integrated protection includes UVLO, UVP, OVP, OCP, OTP, and cycle-by-cycle per-phase current limiting.

When paired with Reed [Smart Power Stages](#) or [Smart Power Blocks](#), the RS19822 provides a scalable, high-density multiphase power solution for demanding processor and graphics core power rails. The device is offered in a 5mm $\times$ 5mm 40-pin QFN package and operates from -40°C to 125°C .



Typical Application Schematic (6 + 2)



Ordering Information

PART NUMBER	PACKAGE	SIZE	MSL RATING	SHIPPING METHOD	PACKAGE MARKING
RS19822R	QFN-40	5 × 5mm		5000u Tape & Reel	R19822

Top Marking



Line 1

- RS: Prefix of Reed Semiconductor (R is replaced by E for engineering lots)
- YY: Year code
- WW: Week code

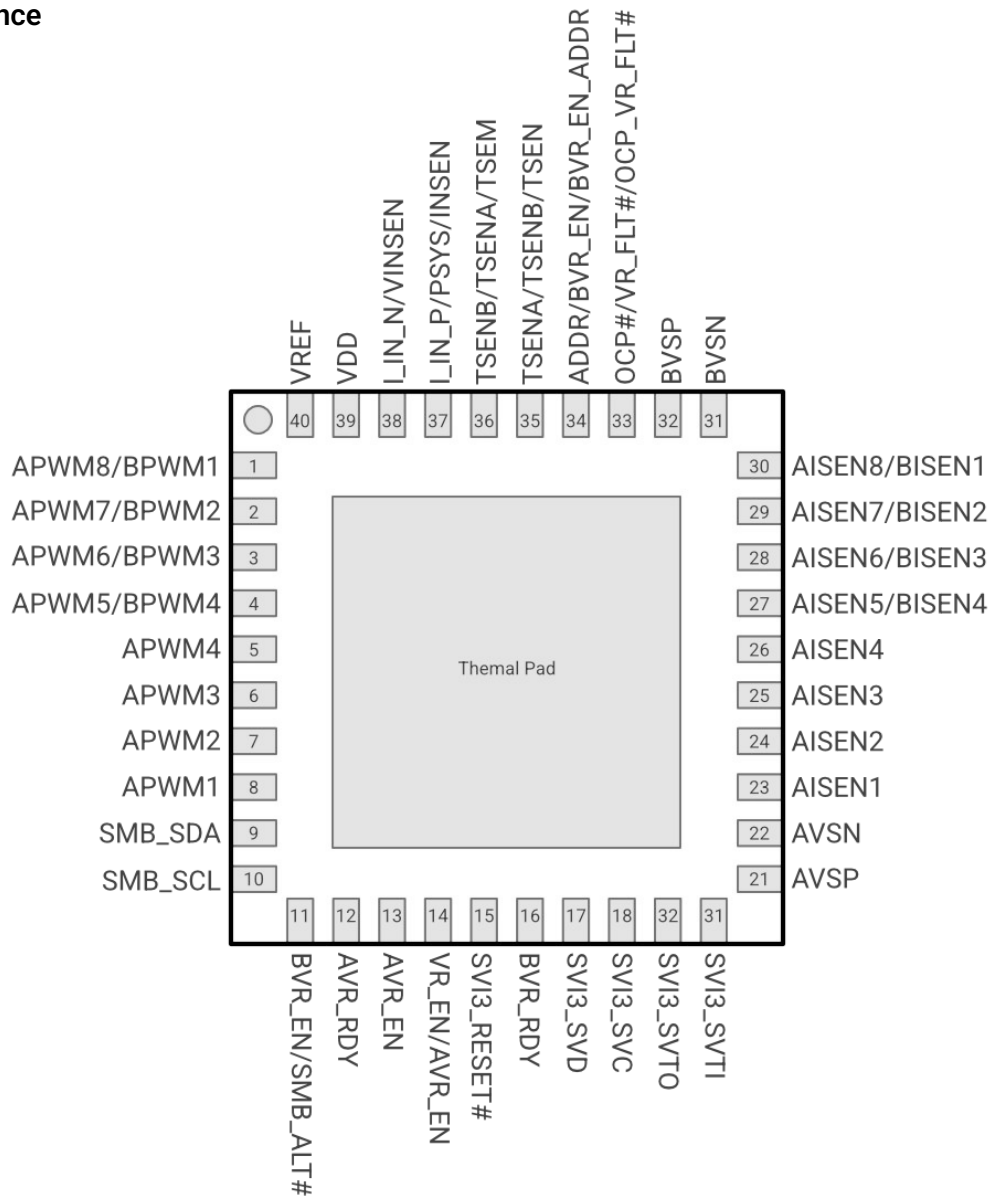
Line 2

- PPPPP: Truncated part number

Line 3

- LLLLL: Lot code
- S: Assembly site code

Package Reference



QFN-40 (5 × 5mm)

Pin Descriptions

PIN	NAME	TYPE	DESCRIPTION
1	APWM8/ BPWM1	O	PWM output for Rail A Phase 8 or Rail B Phase 1.
2	APWM7/ BPWM2	O	PWM output for Rail A Phase 7 or Rail B Phase 2.
3	APWM6/ BPWM3	O	PWM output for Rail A Phase 6 or Rail B Phase 3.
4	APWM5/ BPWM4	O	PWM output for Rail A Phase 5 or Rail B Phase 4.
5	APWM4	O	PWM output for Rail A Phase 4.
6	APWM3	O	PWM output for Rail A Phase 3.
7	APWM2	O	PWM output for Rail A Phase 2.
8	APWM1	O	PWM output for Rail A Phase 1.
9	SMB_SDA	I/O	PMBus bidirectional serial data.
10	SMB_SCL	I	PMBus serial clock input.
11	BVR_EN/ SMB_ALT#	I/O	Multifunction pin configurable through MTP as BVR_EN or SMB_ALT#. BVR_EN: Active-high Rail B enable input. SMB_ALT#: Active-low, open-drain PMBus ALERT# output.
12	AVR_RDY	O	Active-high Power Good output. Asserts when the Rail A output voltage is in regulation.
13	VR_EN/ AVR_EN	I	Multifunction pin configurable through MTP as VR_EN or AVR_EN. VR_EN: Active-high enable input for Rails A and B. AVR_EN: Active-high Rail A enable input.
14	SVI3_RESET#	I	Active-low SVI3 reset input. Resets the SVI3 state machines and SVI3-defined registers to their default states.
15	SVI3_VDDIO	P	SVI3 interface supply input. Provides the I/O reference for SVD, SVTI, and SVTO. Connect a $\geq 1\mu\text{F}$ decoupling capacitor to GND.
16	BVR_RDY	O	Active-high Power Good output. Asserts when the Rail B output voltage is in regulation.
17	SVI3_SVD	I	SVI3 serial VID command data input.
18	SVI3_SVC	I	SVI3 serial VID clock input for SVD, SVTI, and SVTO.
19	SVI3_SVTO	O	SVI3 telemetry output. Carries telemetry and acknowledge packets.
20	SVI3_SVTI	I	SVI3 telemetry input. Receives telemetry and acknowledge packets from the next device in the telemetry daisy chain.
21	AVSP	I	Rail A positive remote-sense input. Connect to the output voltage at the point of regulation.
22	AVSN	I	Rail A negative remote-sense input. Connect to the load ground at the point of regulation.
23	AISEN1	I	Current-sense input for Rail A Phase 1.
24	AISEN2	I	Current-sense input for Rail A Phase 2.
25	AISEN3	I	Current-sense input for Rail A Phase 3.

PWM outputs (Pins 1–8): 3.3V CMOS tri-state outputs. Low: low-side FET ON; High: high-side FET ON; Tri-state: both FETs OFF. If unused, leave floating.

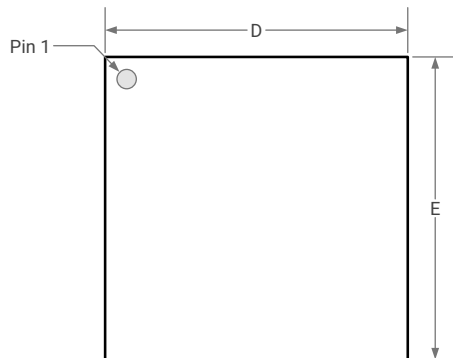
Type: I = Input, O = Output, I/O = Bidirectional, P = Power, G = Ground, – = No Connect.

Pin Descriptions

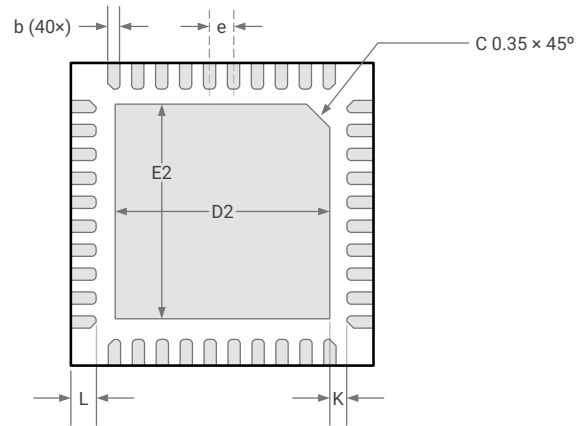
PIN	NAME	TYPE	DESCRIPTION
26	AISEN4	I	Current-sense input for Rail A Phase 4.
27	AISEN5/ BISEN4	I	Current-sense input for Rail A Phase 5 or Rail B Phase 4.
28	AISEN6/ BISEN3	I	Current-sense input for Rail A Phase 6 or Rail B Phase 3.
29	AISEN7/ BISEN2	I	Current-sense input for Rail A Phase 7 or Rail B Phase 2.
30	AISEN8/ BISEN1	I	Current-sense input for Rail A Phase 8 or Rail B Phase 1.
31	BVSN	I	Rail B negative remote-sense input. Connect to the load ground at the point of regulation.
32	BVSP	I	Rail B positive remote-sense input. Connect to the output voltage at the point of regulation.
33	OCP\$/ VR_FLT#/ OCP_VR_ FLT#	O	Multifunction fault output configurable through MTP as OCP#, VR_FLT#, or OCP_VR_FLT#. OCP#: Active-low output that asserts when output current exceeds the configured SVI3 OCP threshold. VR_FLT#: Active-low catastrophic-fault indicator. OCP_VR_FLT#: Combined OCP# and VR_FLT# output.
34	ADDR/ BVR_EN/ BCR_EN_ ADDR	I	Multifunction pin configurable through MTP as ADDR, BVR_EN, or BVR_EN_ADDR. ADDR: PMBus address-select input. Connect to GND and VREF through resistors to set the PMBus address; the address is latched at VDD power-up. BVR_EN: Active-high Rail B enable input. BVR_EN_ADDR: Combined PMBus address-select and Rail B enable input; the address is latched at VDD power-up, after which the pin functions as BVR_EN.
35	TSENA/ TSENB/ TSEN	I	Multifunction temperature-sense input configurable through MTP as TSENA, TSENB, or TSEN. TSENA: Temperature-sense input for Rail A power stages. TSENB: Temperature-sense input for Rail B power stages. TSEN: Temperature-sense input for power stages on Rails A and B.
36	TSENB/ TSENA/ TSEN	I	Multifunction temperature-sense input configurable through MTP as TSENB, TSENA, or TSEN. TSENB: Temperature-sense input for Rail B power stages. TSENA: Temperature-sense input for Rail A power stages. TSEN: Temperature-sense input for power stages on Rails A and B.
37	I_IN_P/PSYS/ IINSEN	I	Multifunction input configurable through MTP as I_IN_P, PSYS, or IINSEN. I_IN_P: Positive input-current sense input. Connect to the positive side of a local current-sense resistor through a 1/6 resistive divider. If input-current sensing is unused, connect I_IN_P and I_IN_N together and bias through a 1/16 resistive divider. PSYS: System input-power sense input. Connect a resistor to GND; do not exceed VREF (1.5V). IINSEN: Input-current sense input. Connect a resistor to GND; do not exceed VREF (1.5V).
38	I_IN_N/ VINSEN	I	Multifunction input configurable through MTP as I_IN_N or VINSEN. I_IN_N: Negative input-current sense input. Connect to the negative side of a local current-sense resistor through a 1/6 resistive divider and decouple with a 0.1µF capacitor to GND. Also functions as the power-stage input-voltage sense input. VINSEN: Power-stage input-voltage sense input. Connect to the input voltage through a 1/6 resistive divider and decouple with a 0.1µF capacitor to GND.
39	VDD	P	3.3V supply input. Connect a 1µF or larger ceramic bypass capacitor to GND.
40	VREF	O	1.5V reference-voltage output. Connect a 1µF to 4.7µF decoupling capacitor to GND.
—	Thermal Pad	G	Exposed thermal pad. Connect to the GND plane with multiple thermal vias.

Type: I = Input, O = Output, I/O = Bidirectional, P = Power, G = Ground, — = No Connect.

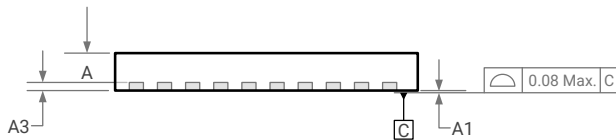
Package Dimensions



TOP VIEW



BOTTOM VIEW



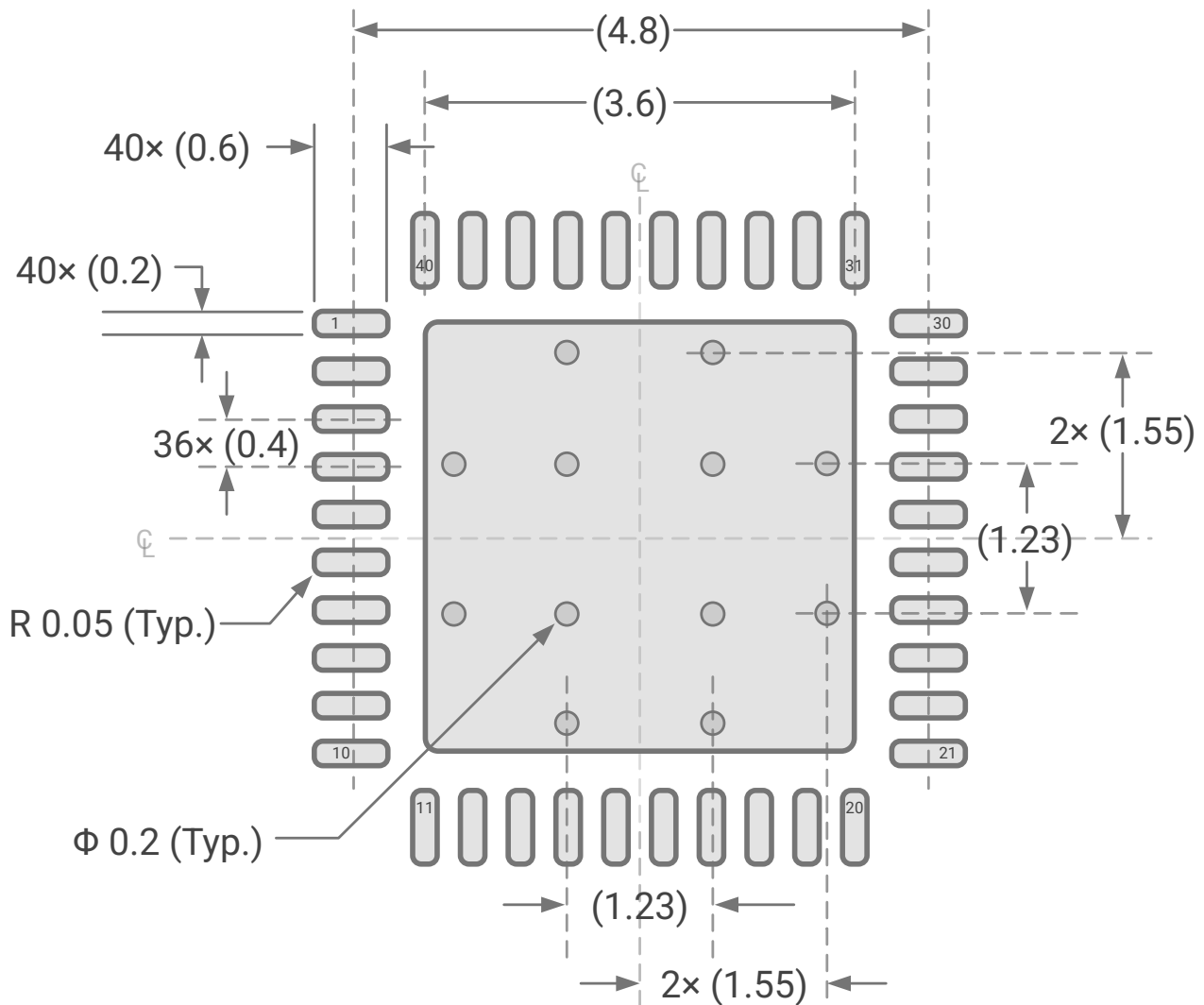
SIDE VIEW

REF	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 Ref.		
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.55	3.60	3.65
E2	3.55	3.60	3.65
b	0.15	0.20	0.25
e	0.40 BSC		
L	0.35	0.40	0.45
K	0.20	—	—

Notes

1. All dimensions are in millimeters.
2. Lead coplanarity shall be 0.1mm maximum.
3. Drawing is not to scale.

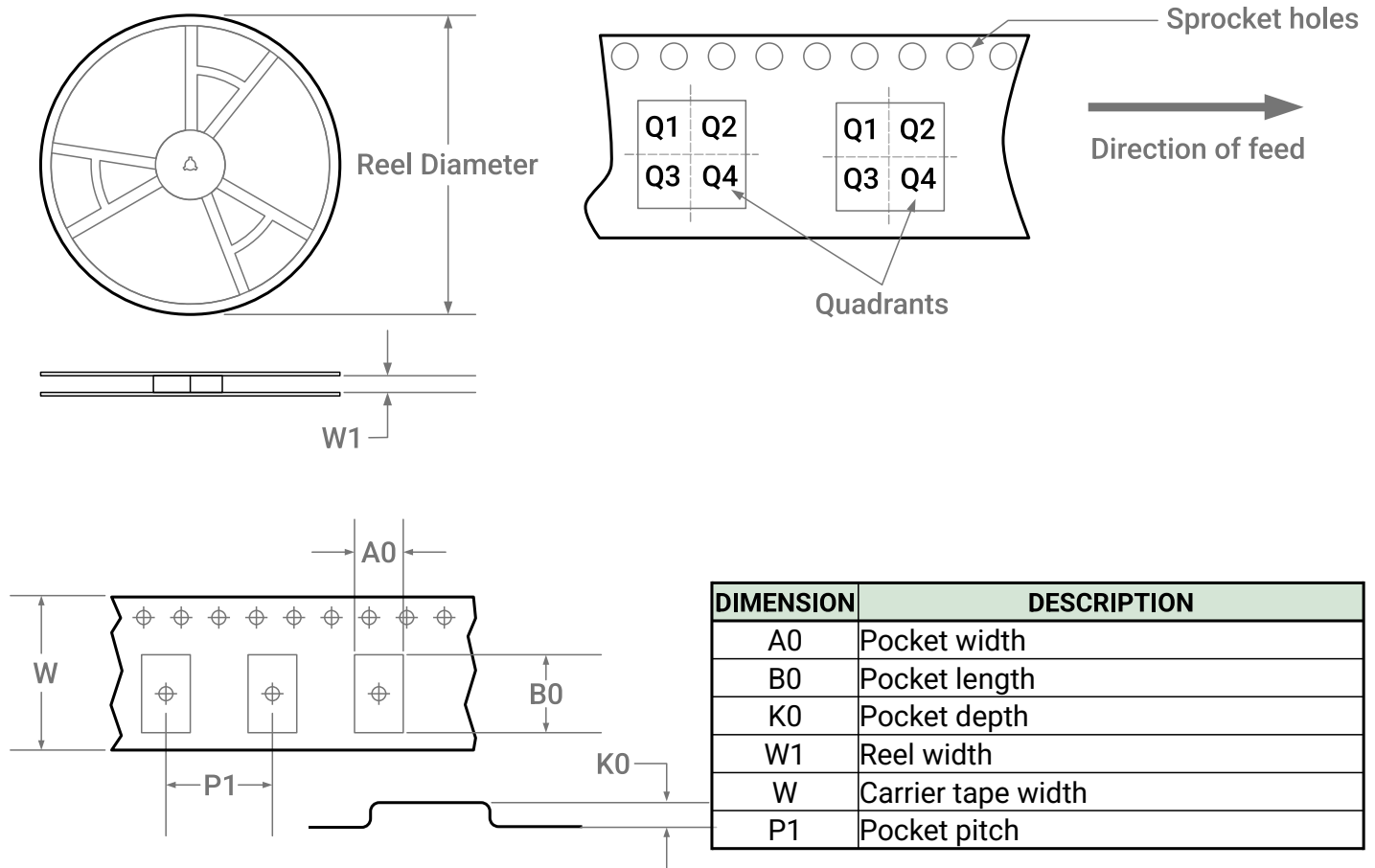
Recommended Land Pattern



Note:

1. All dimensions are in millimeters.
2. Drawing is not to scale.

Tape and Reel Information

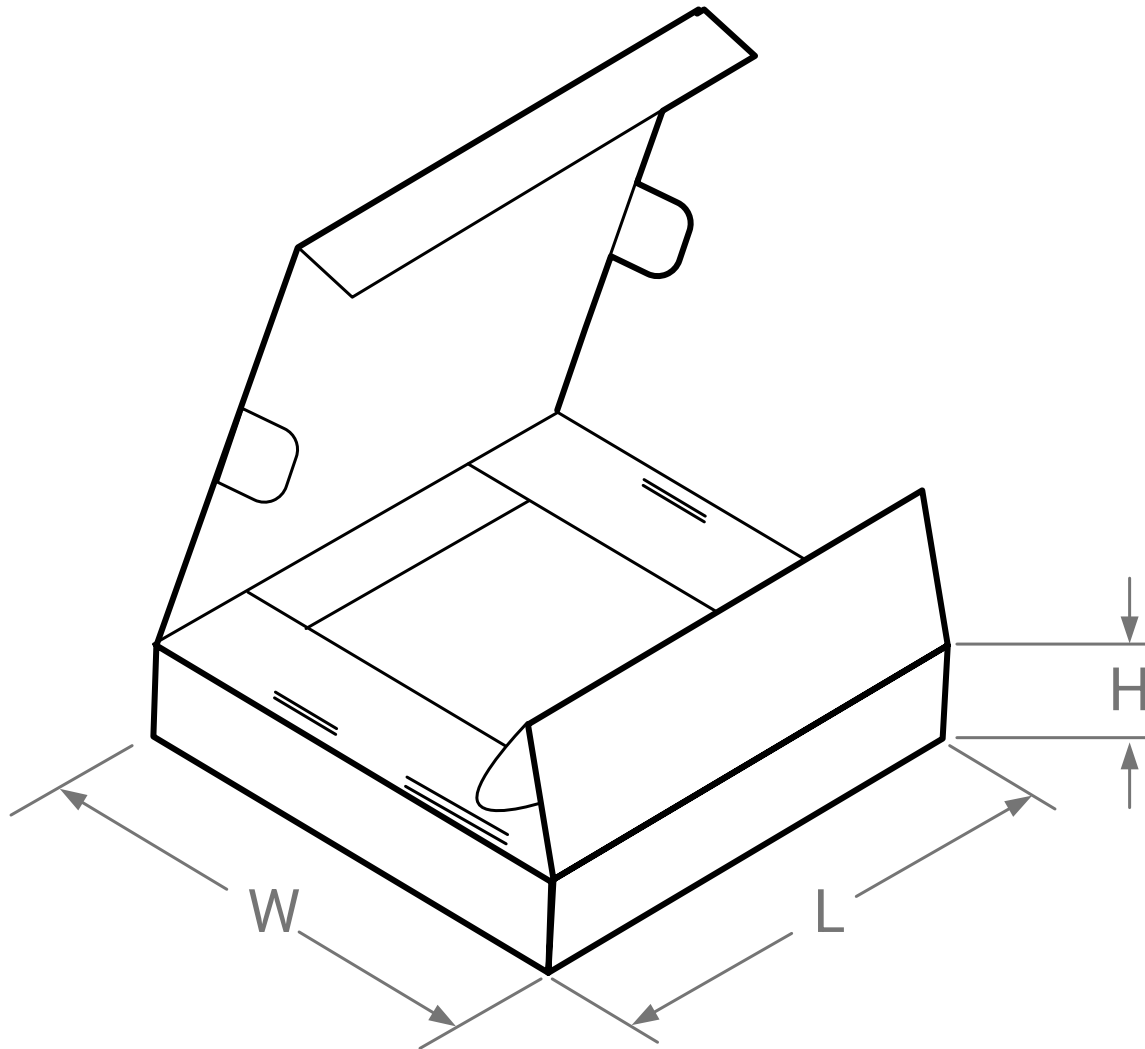


PACKAGE SIZE	REEL DIAMETER	W1	A0	B0	K0	P1	W	QUADRANT
5 × 5	330	12.8	5.25	5.25	1.10	8.00	12.00	Q2

Note:

1. All dimensions are nominal
2. All dimensions are in millimeters (mm)

Pizza Box Dimensions



PACKAGE SIZE	UNITS / BOX	LENGTH	WIDTH	HEIGHT
5 × 5	5000	367	367	38

Notes:

1. All measurements are in millimeters;
2. All measurements are nominal.